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(54) **Method and circuit for scanning capacitive loads.**

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Description

The present invention relates to a scanning method and a scanning circuit and, more particularly, to a scanning method and a scanning circuit which use a display element of a liquid crystal or the like and are suitable for an active matrix type display having a driver built therein.

The so-called "active matrix display", which is formed on a substrate of glass or the like with switching elements such as thin film active elements, e.g., diodes or thin film transistors (which will be referred to as the "TFTs" for brevity) and which are combined with a substance having the electro-optical effect such as a liquid crystal, is featured by capability of forming a large-area, high-fineness and high-quality display. In addition, the display using the TFTs constitutes a driver of the TFTs so that it forms on the glass substrate not only a display unit but also a circuit for driving the display unit to reduce the number of connecting lines from the outside and the number of external drivers. This makes it possible to drop the production cost and to prevent the reliability from dropping due to inferior connection. Thus, many displays having the driver built therein are proposed in Japanese Patent Laid-Opens JP-A-5692573 and JP-A-57100467 and so on since they have been proposed in Proceedings of IEEE, 59, P1566 (1971). These circuit structures can constitute a signal circuit for generating a signal voltage to be applied to the wiring at a signal (or data) side, of a smaller number of TFT elements per line but still has room for improvements in the following points. First of all, the voltage applied to the signal electrode (or data line) of the display unit has its signal voltage applied to the signal electrode through a TFT element at the output step of a driver, when the TFT element is on. When the TFT element is then turned off, the voltage is held by the capacitor $C\ell$ of the signal electrode. These operations are accomplished for a period, in which one of the scanning lines is selected so that a scanning voltage for turning on the TFT element of the display unit is applied to the scanning electrode. This makes it necessary for the voltage applied to the signal electrode for that period to be held till the end of the scanning period of the one line. If the insulating resistance of the signal electrode to another unit is insufficient, the voltage applied to the signal electrode capacitor till the end of the scanning period is released so that the voltage applied to the TFT of a pixel unit drops. As a result, each pixel connected with that signal electrode has an uneven luminance for each signal electrode because the applied voltage is always low. In order to prevent this, the TFT element at the output step of the driver should be held on till the end of the scanning period of one line so that an electric current may be supplied to an extent corresponding to the discharge of the voltage from the signal electrode.

Next, it is necessary to consider the problems of the ON characteristics of the TFT elements of the display unit and the output step. As the display takes the higher capacity, i.e., the larger area and the more scanning lines, the scanning periods of one line and one pixel become the shorter. Since the electrostatic capacity per line becomes the higher, on the contrary, a relatively higher electrostatic capacitive load has to be charged up for a short period for either a so-called "sequential dot scanning method", by which signal lines are sequentially scanned by one signal line for one scanning period, or a scanning method of sequentially scanning by a plurality of signal lines (the latter method will be called the "sequential block scanning method by making one block of a plurality of lines to be once scanned). The TFT element at the output step of the driver should also have a high mutual drain conductance gm. According to the aforementioned scanning methods, moreover, the ON voltage of the TFT elements of the display unit are so shortened that an insufficient voltage is applied to the liquid crystal to drop the contrast ratio of the display. This makes it necessary to enlarge the channel width W of the TFT elements thereby to increase the mutual conductance gm. As a result, the circuit area is increased, and the ratio occupied by the display electrode of the display unit is reduced together with the display characteristics. In order to avoid this, the so-called "sequential line scanning method", by which the TFT element of the display unit is turned on for the substantially whole address period of one scanning line with the signal voltage being applied, is desired as the driving method.

Next, the structure of a built-in driver or a driver at a signal side (or data voltage generating side) is required to have high-speed operations so that cares should be taken of the circuit design. If the number of the pixels of the display unit of a display is assumed to be expressed by P (i.e., the number of vertical pixels) x Q (i.e., the number of horizontal pixels) and if the frequency for rewriting one frame (which will be called the "frame frequency") is denoted at f_F (Hz), for example, the maximum frequency f_{max} of a signal voltage inputted to the display is calculated by P x Q x f_F. With the pixel number of the display unit being P = 400, Q = 640 x 3 (assuming the display of three colors R, G and B) and f_F = 60 Hz, for example, the maximum frequency f_{max} takes such a very high value as is expressed by $f_{max} = 46.08 \times 10^6$ Hz = 46.08 MHz. Since the circuit operating within such frequency band is very difficult to be constructed of TFTs of amorphous or polycrystalline silicon, for example, it is necessary to improve the circuit structure or the signal applying method having characteristics matching the TFT elements. The above-specified example of the prior art is a circuit structure which has been devised to apply input data in parallel thereby to drop the aforementioned maximum frequency f_{max} with the number of

the input data. However, the part for receiving the signals from the outside and the part for applying the input signals to the display unit are of the voltage distribution type resorting to the electrostatic capacity, in which the common TFT elements are used or in which the TFT elements are used as transfer gates. As a result, the example of the prior art requires the TFT elements of the input part to drive a high electrostatic capacitive load so that it is defectively difficult to respond to an input signal of high frequency.

In the aforementioned embodiment, moreover, the timing for applying or the circuit structure for generating the drive voltage such as scanning pulses for operating the TFT elements for processing the input data signals divides the selection period of one scanning line with the number of blocks, each of which is composed of a plurality of signal lines. Since the pulse width of the scanning pulses becomes the smaller for the larger frame and the higher fineness, a circuit for generating the scanning pulses is required of high-speed operations.

The prior art thus far described has failed to take considerations in efficiently processing the high-speed input data of a built-in signal driver using TFTs to apply them to the display unit so that it has been troubled in its own operating speed and the displaying characteristics of the display unit.

The present invention seeks to provide high-speed scanning method and circuit which can use a semiconductor element capable of switching at a relatively low speed even in case input data at a high rate.

According to a first aspect of the present invention there is provided a method of scanning an array;

the array comprising:

K ($K \geqq 3$) consecutive semiconductor switch elements connected to at least one further switch element each of said consecutive switch elements having a first main electrode connected to said at least one further switch element, a second main electrode, and a control electrode responsive to a control signal for controlling the transmissive and intransmissive states between the first and second main electrodes;

said at least one further switch element being responsive to at least one further control signal for controlling the transmissive and intransmissive states of said at least one further switch element between at least one input signal and the consecutive switch elements; and

capacitive loads connected respectively to the second main electrodes of each of said consecutive semiconductor switch elements;

the method comprising:

repeatedly scanning the array with a predetermined scanning period, the scanning of the array including causing each of the K consecutive semiconductor switch elements to have at least one transmissive period and at least one intransmissive period, during which transmissive period the at least one input signal is applied to the corresponding capacitive load wherein:

the time for which a selected number L ($K > L \geqq 2$) of adjacent ones of the consecutive semiconductor switch elements are all rendered transmissive and the time for which said selected number of semiconductor switch elements are all rendered intransmissive are included in a period which is less than said predetermined scanning period, and that the total duration of one transmissive period and one intransmissiveperiod of any one of the K consecutive semiconductor switch elements is also less than said predetermined scanning period.

According to a second aspect of the present invention there is provided a method of scanning an array;

the array comprising:

K ($K \geqq 3$) consecutive semiconductor switch elements each having a first main electrode responsive to an input signal, a second main electrode, and a control electrode responsive to a control signal for controlling the transmissive and intransmissive states of the input signal between the first and second main electrodes; and

capacitive loads connected respectively to the second main electrodes of each of said consecutive semiconductor switch elements;

the method comprising:

repeatedly scanning the array with a predetermined scanning period, the scanning of the array including causing each of the K consecutive semiconductor switch elements to have at least one transmissive period and at least one intransmissive period, during which transmissive period the input signal is applied to the corresponding capacitive load wherein:

the time for which a selected number L ($K > L \geqq 2$) of adjacent ones of the consecutive semiconductor switch elements are all rendered transmissive and the time for which said selected number L of semiconductor switch elements are all rendered intransmissive are included in a period which is less than said predetermined scanning period, and that the total duration of one transmissive period and one intransmissive period of any one of the K consecutive semiconductor switch elements is also less than said predetermined scanning period.

According to a third aspect of the present invention there is provided a scanning circuit having:

an array comprising:

K ($K \geqq 3$) consecutive semiconductor switch elements connected to at least one further switch element, each of said consecutive switch elements having a first main electrode connected to said at least one further switch element, a second main electrode, and a control electrode responsive to a control signal for controlling the transmissive and intransmissive states between the first and second main electrodes;

capacitive loads connected respectively to the second main electrodes of each semiconductor switch elements;

said at least one further switch element being responsive to at least one further control signal for controlling the transmissive and intransmissive states of said at least one further switch element between at least one input signal and the consecutive switch elements;

an input signal source for generating said at least one input signal for said further semiconductor switch elements; and

a control circuit for generating said control signal of said semiconductor switch elements said control circuit being arranged to generate said control signals sequentially so as repeatedly to scan the array with a predetermined scanning period, the scanning of the array including causing each of the K semiconductor switch elements to have at least one transmissive period and at least one intransmissive period, during which transmissive period the input signal is applied to the corresponding capacitive load wherein:

the control circuit is arranged such that the time for which a selected number L ($K > L \geqq 2$) of adjacent ones of the consecutive semiconductor switch elements are all rendered transmissive and the time for which said selected number of semiconductor switch elements are all rendered intransmissive are included in a period which is less than said predetermined scanning period, and that the total duration of one transmissive period and one intransmissive period of any one of the K consecutive semiconductor switch elements is also less than said predetermined scanning period.

According to a fourth aspect of the present invention there is provided a scanning circuit having:

an array comprising:

K ($K \geqq 3$) consecutive semiconductor switch elements each having a first main electrode responsive to an input signal, a second main electrode, and a control electrode responsive to a control signal for controlling the transmissive and intransmissive states of the input signal between the first and second main electrodes;

capacitive loads connected respectively to the second main electrodes of each of said consecutive semiconductor switch elements;

an input signal source for generating said input signals of said semiconductor switch elements; and

a control circuit for generating said control signals of said semiconductor switch elements, said control circuit being arranged to generate said control signals sequentially so as repeatedly to scan the array with a predetermined scanning period, the scanning of the array including causing each of the K semiconductor switch elements to have at least one transmissive period and at least one intransmissiveperiod, during which transmissive period the input signal is applied to the corresponding capacitive load wherein:

the control circuit is arranged such that:

the time for which a selected number L ($K > L \geqq 2$) of adjacent ones of the consecutive semiconductor switch elements are all rendered transmissive and the time for which said selected number of semiconductor switch elements are all rendered intransmissive are included in a period which is less than said predetermined scanning period, and that the total duration of one transmissive period and one intransmissive period of any one of the K consecutive semiconductor switch elements is also less than said predetermined scanning period.

Preferably the semiconductor switch elements are arranged in the array in J ($J \geqq 1$) blocks, each block including M ($M \geqq 3$; $K = J \times M$) semiconductor switch elements.

Then the times for which the semiconductor switch elements at the boundary of adjacent blocks are rendered transmissive overlap partially but not fully;

and

the times for which at least two semiconductor switch elements of each block are rendered transmissive overlap partially but not fully.

It should be noted that EP-A-0213630 (which comes within the scope of EPC Article 54(3)) discloses a method in which the time for which a selected L ($K > L \geqq 2$) of the semiconductor switch elements of adjacent scans are all rendered transmissive and the time for which said semiconductor switch elements are all rendered intransmissive are included in a period which is not greater than the scanning period. However, in this prior art, the total direction of one transmissive period and one intransmissive period of any one of the K semiconductor switch elements equals said scanning period and thus is not less than this period.

Other features of the present invention will become apparent from the following description taken in connection with the embodiments thereof with reference to the accompanying drawings, in which:

Figs. 1, 2, 7, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 20, 21, 22, 23 and 24 are circuit diagrams showing the embodiments of the present invention;

Fig. 3 is a circuit diagram and a characteristic diagram illustrating an inverter; and

Figs. 4, 5, 6, 8 and 19 are drive waveform charts.

The principle of the present invention will be described in the following with reference to Figs. 18 and 19. Fig. 18 is a circuit diagram for illustrating the principle of the present invention, and Fig. 19 is a time chart of the circuit of Fig. 18.

In Fig. 18, reference numerals 101 to 104 denote four ($K = 4$) n-channel type MOS transistors exemplifying semiconductor switches, preferably thin film transistors (which will be referred to as the "TFTs" for brevity) formed in a single block ($J = 1$; $M = K$) on a

glass substrate. One main electrode of each of the TFTs 101 to 104 is commonly responsive to a continuous input signal V_{in} such as analog or digital image signals. The other main electrode of each of the TFTs 101 to 104 is connected with each of capacitive loads 201 to 204, respectively. These capacitive loads 201 to 204 are preferably exemplified by liquid-crystal wiring capacitors or the input gate capacitors of MOS transistors of a next stage. The control electrodes of the TFTs 101 to 104 are made responsive to scanning pulses ϕ_1, ϕ_2, ϕ_3 and ϕ_4 of first and second potential levels V_1 and V_2 or control signals for controlling the ON and OFF states, in which the input signals V_{in} are transmissive and intransmissive, respectively, from one main electrode to the other main electrode. Here, for example, the first potential level V_1 is at the ground potential (at 0 V), and the second potential level V_2 is at the supply potential (at V_{cc} = 5 V).

In Fig. 19, at a time t_1, the pulses ϕ_1 transfer from the level V_1 to the level V_2, and the TFT 101 transfers from the OFF state to the ON state so that the input signal V_{in} is applied, as the voltage V_{201} of the capacitive load 201, to the capacitive load 201.

At a time t_2, the pulses ϕ_1 are invaried and remains at the level V_2 so that the TFT 101 is held in the ON state. At this time, the pulses ϕ_2 vary from the level V_1 to the level V_2, and the TFT 102 transfers from the OFF state to the ON state so that the input signal V_{in} is applied, as the voltage V_{202} of the capacitive load 202, to the capacitive load 202.

At a time t_3, the pulses ϕ_1 vary from the level V_2 to the level V_1, and the TFT 101 transfers from the ON state to the OFF state so that the capacitive load 201 holds the value of the input signal V_{in} in the just preceding ON state of the TFT 101 for a predetermined period. At this time, that value may slightly drop due to the presence of a leakage resistance. The pulses ϕ_2 is invaried and remains at the level V_2 so that the TFT 102 holds the ON state. For the period from the time t_2 to the time t_3, more specifically, the pulses ϕ_1 and ϕ_2 of adjoining scans are at the level V_2, and the two (L = 2) TFTs 101 and 102 are in the ON state so that the input signal V_{in} is applied to the two. At the same time, the pulses ϕ_3 and are ϕ_4 the level V_1, and both the TFTs 103 and 104 are in the OFF state. At the time t_3, on the other hand, the pulses ϕ_3 vary from the level V_1 to the level V_2, and the TFT 103 transfers to the ON state so that the input signal V_{in} is applied, as the voltage V_{203} of the capacitive load 203, to the capacitive load 203.

At a time t_4, the pulses ϕ_1 is invaried and remains at the level V_1, and the TFT 101 holds the OFF state. The pulses ϕ_2 vary from the level V_2 to the level V_1, and the TFT 102 transfers from the ON state to the OFF state so that the capacitive load 202 holds the value of the input signal in the just preceding ON state of the TFT 102 for a predetermined period. The pulses ϕ_3 is invaried and remains at the level V_2, and the TFT 103 maintains the ON state. The pulses ϕ_4 vary from the level V_1 to the level V_2, and the TFT 104 transfers from the OFF state to the ON state so that the input signal V_{in} is applied, as the voltage V_{204} of the capacitive load 204, to the capacitive load 204.

For the period from the time t_3 to the time t_4, more specifically, the pulses ϕ_2 and ϕ_3 are at the level V_2, and the two (L = 2) TFTs 102 and 103 of adjacent scans are in the ON state. On the other hand, both the pulses ϕ_1 and ϕ_4 of adjacent scans are at the level V_1, and both the TFTs 101 and 104 are in the OFF state.

At a time t_5, the pulses ϕ_1 vary from the level V_1 to the level V_2 as at the time t_1. For the period from the instant t_4 to the time t_5, the pulses ϕ_1 and ϕ_2 of adjacent scans are at the level V_1, and the two (L = 2) TFTs 101 and 102 are in the OFF state. At the same time, both the pulses ϕ_3 and ϕ_4 are at the level V_2, and the two TFTs 103 and 104 are in the ON state. Similar operations are repeated on and on at times t_6, t_7 and so on.

The period from the time t_1 to the time t_5 is one period, for which the scanning signals ϕ_1 to ϕ_4 vary sequentially from the level V_1 to the level V_2 so that the TFTs 101 to 104 transfer sequentially from the OFF state to the ON state. For this one period, moreover, the scanning signals ϕ_1 to ϕ_4 vary sequentially from the level V_2 to the level V_1 so that the TFTs 101 to 104 transfer sequentially from the OFF state to the ON state. Incidentally, in Fig. 11, the durations of the periods from the time t_1 to the period t_2, from the time t_2 to the time t_3, from the time t_3 to the time t_4, and from the time t_4 to the time t_6 are substantially equal, but may be different.

Since the scanning signals ϕ_1 to ϕ_4 thus overlap one another, their respective substantial frequencies are reduced so that they can be produced even if the TFTs 101 to 104 do not have such high-speed switching characteristics. In other words, high-speed scanning signals can be produced without varying the switching characteristics of the TFTs 101 to 104.

Incidentally, Fig. 19 presents an example in which M = 4 and L = 2 so that M = 2L. In case M is an odd number, however, it is preferable to set either M = 2L - 1 or M = 2L + 1.

Another embodiment of the present invention will be described with reference to Fig. 1.

Fig. 1 shows a plane type display which is constructed, by TFT elements formed on a transparent insulating substrate 16 made of such as glass or plastics, of: a number of pixels 18 of a display unit; a plurality of scanning electrodes 15 for driving the individual pixels; a plurality of signal electrodes 12; a scanning circuit 14; and a signal circuit having the following structure. Each of the pixels 18 is composed of a TFT element 18-1, and an inter-electrode display element 18-2 of a liquid crystal or the like to be driven by the TFT element 18-1.

As a component of the signal circuit, one block is

prepared by connecting a plurality of TFT elements, in which a signal input wire 1 for feeding displaying data signals including video signals for displaying a TV set is connected with a drain electrode (wherein the TFT element is of an n-channel structure having its one input side main electrode called the "drain" and its other output side main electrode called the "source". Structurally speaking, the TFT element can have its source and drain electrodes formed absolutely symmetrically, and hence the source and drain are named merely for illustrative conveniences.), with at least two gate electrodes (which are the three (M = 3) control electrodes in Fig. 1). The gate 4 of each of the K-number of blocks is connected with a scanning voltage generator 3 for generating the scanning voltage signals ϕ_1, ϕ_2, ϕ_3, - - -, and so on for scanning the respective blocks. In the blocks, the source electrodes of the TFT elements 2 are connected with the drain electrodes of data-sampling TFT elements 6, respectively, which have their gate electrodes connected with a data-sampling wire group 5. The source electrodes of the data-sampling TFTs are connected with data-holding electrostatic capacitors 7 and the drain electrodes of data-transferring TFT elements 10. In the present embodiment, the data-sampling TFTs 6 correspond to the TFT 101 and so on of Fig. 18, and the data-holding electrostatic capacitors 7 correspond to the capacitive loads 201 and so on of Fig. 18. With the source electrodes of the TFT elements 10, there are connected buffers 11 which issues outputs for driving the grouped signal electrodes of the display unit.

The structure of this signal circuit will be classified in terms of its operations: TFT elements 2, the TFT elements 6 and the.accompanying signal lines constitute the signal input sampling circuit; the TFT elements 6 and the electrostatic capacitors 7 constitute a hold circuit; the TFTs 10 constitute a data transfer circuit; and the buffers 11 constitute the driver of the display unit.

The circuits 3 and 14 are those for generating a scanning voltage for scanning one block or line sequentially and are constructed essentially of a shift register and, if necessary, a level converter or an output step buffer circuit. On the other hand, the buffers 11 are circuits for amplifying or impedance-converting the voltage, which is applied to and held in the electrostatic capacitor existing at its input stage, and for applying the same to the display unit and are constructed of a variety of circuits represented by inverters.

Fig. 2 shows a modification of the circuit of Fig. 1. The signal V_v applied to the signal input wire 1 is switched for each block by the single TFT element 2 and is applied to the TFT elements 6. The number of these TFT elements can be reduced to improve the reliability.

Fig. 3 plots the characteristics of an output voltage V_{out} against the input voltage V_{in} of an inverter circuit. These characteristics correspond to the case of the so-called "E/E type inverter, in which the TFT element is made of polycrystalline silicon and in which the circuit structure of the inverter uses two enhancement type TFTs. There exists a region in which the output voltage V_{out} varies generally linearly with respect to the input voltage V_{in} and which is used as the operating region of the buffer. In the regions of input voltages V_{in1} and V_{in2} of Fig. 2, more specifically, output voltages V_{out1} and V_{out2} linearly vary. The gradient of that portion and the bias voltage value against the input voltage value vary depending upon the characteristics of the TFT element and the circuit design constants such as an inverter ratio, and it is sufficient that the driving conditions be so determined as to set the portion of the linear region as the operating region. Generally speaking, the TFT element is one having the MOS structure, and the gate input impedance is sufficient high. As a result, the use of the inverter circuit shown in Fig. 3 as the buffers 11 releases none of the charges held in the input portion through the input portion of the buffers 11 so that the signals transmitted from the transfer gates 10 are satisfactorily held.

Fig. 4 presents the waveforms of the drive voltages to be applied to the individual portions of Fig. 1. The waveforms belong to scanning voltages V_{SC1}, V_{SC2}, V_{SC3}, - - -, and so on, a video input signal V_v to be applied to the pixel of each scanning electrode, the voltage signals ϕ_1, ϕ_2, ϕ_3, - - -, and so on, clock pulses CP_1, CP_2 and CP_3 to be applied to the gates of the TFT elements 6 for sampling the data from each block, and a voltage V_{st} for transferring the data voltage held in the data-storing electrostatic capacitors 7 to the buffer portion. The video signal V_v is sampled by the electrostatic capacitors 7 through TFT2 and TFT6 when both TFT2 and TFT6 are turned on by any of the voltage signals ϕ_1, ϕ_2, ϕ_3, - - -, and so on and the clock pulses CP_1, CP_2, and CP_3 are applied. In case either TFT 2 or the TFT 6 is turned off, on the contrary, the voltages of the electrostatic capacitors 7 are held. It takes place only once for one scanning line period that both the TFT 2 and the TFT 6 of the combinations of the scanning voltages ϕ and the clock pulses CP are turned on. As a result, the video signal V_v is sequentially stored in the electrostatic capacitors at the lefthand side of Fig. 1. It goes without saying that the video signal V_v can be stored from the electrostatic capacitors at the righthand side by inverting the applying direction of the scanning voltages ϕ and the applying order of the clock pulses CP. At this time, the characteristics of the TFTs 2 and 6 determine the OFF resistances such that the capacitors 7 are charged up while the clock pulses CP_1, CP_2 and CP_3 are ON and such that the voltages of the capacitors 7 are held for the OFF period. The OFF period assumes its maximum at the signal line of the most

lefthand end in the case of Fig. 1 and is substantially equal to one scanning period. The ratio of the ON period and the OFF period is substantially equal to the value of Q in the display having Q pixels in the horizontal direction. Since Q is about 2,000, for example, the ON/OFF ratio of the TFT elements is sufficient for the charging and holding operations. Next, the voltages to be applied to the input portions of the buffers 11 are determined by the capacitance division of the input capacitors of the capacitors 7 and the buffers 11. Therefore, it is sufficient that the capacitance of the capacitors 7 be set higher than the input capacitance of the buffers. In the embodiment of the prior art having no buffer, the capacitors 7 have had to take a larger value than that of the electrostatic capacitors attached to the signal electrodes so that the TFT 2 and the TFT 6 have found it difficult to charge the capacitors 7 at a high rate. In the present embodiment, on the contrary, the capacitors 7 do not take such high values that they can be charged at a high speed by the TFT 2 and TFT 6.

On the other hand, the outputs of the buffers can apply the voltages to the signal electrodes during the scanning period of about one horizontal line except the fly-back period. Even in case the insulating resistances between the signal electrodes and the scanning electrodes disperse or in case the insulating resistances of the gate insulating films of the TFT elements of the display unit disperse, the currents can be supplied by the buffers so that the voltages of the signal electrodes can be easily held constant to prevent the unevenness of the display.

Moreover, the operating speed of the circuits for generating the scanning voltages ϕ_1, ϕ_2 and ϕ_3 can be dropped by the number of the TFTs 2 in one block, as compared with the case of the sequential dot scanning operation. The embodiments shown in Figs. 1 and 2 are constructed by using the three TFT elements in one block. The operating frequency of the circuit 3 can be dropped by increasing the number of the TFT elements so that the circuits can be easily built in by the TFT elements.

In the present embodiment, furthermore, the analog signals of the input signals are applied via the single input terminal so that the input signals need not be subjected at the outside to a complicated signal processing such as series/parallel conversions, thus simplifying the circuit structure of the outside.

Fig. 5 presents a modification of the driving waveforms of Fig. 4. In this modification, the DC voltage is applied as the voltage V_v, and the video signal voltages are applied to a common wiring 8 of the electrostatic capacitors 7. Since the voltage of the electrostatic capacitors 7 is determined by the voltage difference between the source electrodes of the sampling TFTs 6 and the common wiring 8 so that the voltage similar to that of Fig. 3 (but having its polarity inverted) can be applied to the capacitors 7.

Fig. 6 presents a modification of the waveforms of Figs. 4 and 5. In case a liquid crystal such as a twisted nematic (TN) liquid crystal is to be driven, the driving voltages are alternating so that waveforms having a reduced DC component have to be applied. In the display using the TFTs, the applied voltage to each pixel has to have its positive and negative polarities inverted for each frame. As this inverting method, there has been proposed a method of inverting the polarities of the signals for each frame or a method of inverting the polarities of the signals for each scanning line. In either method, it is necessary to generate the signal voltages which have polarities inverted around a certain level. Fig. 6 shows an example in which the applied voltages are switched between the voltages V_v and V_b for each scanning line to generate the waveforms so that the voltage difference V_c (equal to V_v - V_b) of the electrostatic capacitors 7 may be inverted for each scanning line. The switching of the voltage voltages V_v and V_b may be caused for each frame. In this case, it is possible to generate voltages which have their polarities inverted for each frame.

Thus, the circuit structure of the present embodiment is featured by the fact that it can easily generate the signal voltages having the input voltages inverted.

Fig. 7 shows the structure which is different from that of Fig. 1 or 2 in that the number of the signal lines in one block are twiced to 6 (M = 6). As compared with the structure of Fig. 1 or 2, the block scanning voltages ϕ_1, ϕ_2, - - -, and ϕ_k can reduce their frequencies to one half (with the twiced pulse width). For the larger number of the signal lines in one block, it is possible to realize the lowering of the frequencies of the block scanning voltages ϕ_1, ϕ_2, - - -, and so on.

Next, in the structure of Fig. 7, the waveforms of the voltages CP_1, CP_2, - - -, and CP_6 corresponding to the sampling voltages CP_1, CP_2 and CP_3 of Fig. 4 are presented in Fig. 8. The embodiment of Fig. 8 is featured by establishing a period for which the adjacent pulses CP_1 and CP_2, CP_2 and CP_3, - - -, or CP_5 and CP_6 overlap each other. Since the voltages to be held at the capacitors 7 connected with the outputs of the TFTs 6 remain at the level as is just before the sampling voltages CP_1, CP_2 and CP_3 assume the level V_3 (or preferably the ground potential = 0), the sampling voltage V_4 (or preferably the supply potential (V_{cc} = 5 V)) may be applied for the preceding period. In other words, the pulse width of the sampling voltages is enlarged the more from that of Fig. 8(a) to those of Fig. 8(b) and 8(c). The restrictions upon the operating speed of a data sampling voltage generator 13 are highly loosened to facilitate the circuit design and to provide room for the characteristics of the TFT elements.

Fig. 9 shows an example of the circuit structure for generating the waveforms presented in Fig. 8. Fig. 9(a) corresponds to the structure of an ordinary shift

register circuit. A six-stage shift register is used for generating the six sampling voltages CP_1, CP_2, - - -, and CP_6. In the structure of Fig. 9(a), the input voltage V_{st} may be elongated so as to elongate the output pulses. Fig. 9(b) corresponds to the structure using two-way shift registers. The overlapping sampling voltages CP_1, CP_2, - - -, and CP_6 are generated by shifting the voltages V_{st1} and V_{st2} by a half pulse to operate the individual shift registers with a one-half frequency of Fig. 9(a). Moreover, Fig. 9(c) corresponds to the structure using three-way shift registers. These shift registers can be operated with a one-third frequency of Fig. 9(a).

Fig. 9 shows the structures using the shift registers. It goes without saying that similar waveforms can be generated even by using a circuit such as a flip-flop.

Since the sampling voltages can have their frequencies lowered with the driving method and circuit structure thus far described, the circuit can easily be constructed by using the TFTs.

On the other hand, the block scanning voltages ϕ_1, ϕ_2, - - -, and so on can also have their pulse widths enlarged, as shown in Figs. 8(a), 8(b) and 8(c), by a method similar to the aforementioned ones. As shown in Fig. 10, the operating frequency of the shift registers can be dropped by the structure of Fig. 10(b) having two-way shift registers, as is different from the structure of Fig. 10(a) of the prior art using one-way shift registers.

Fig. 20 shows one example of the circuit structure for realizing Fig. 9(b). Waveforms in which the phase of the pulses CP_1 and CP_2 is shifted from that of the pulses CP_3 and CP_4 can be outputted by providing two stages of shift registers operating with two-phase clocks and by inverting the phases of the clock pulses.

Fig. 21(a) shows the same circuit structure as that of Fig. 20, in which the clock lines and the supply lines are made common.

The waveforms of these circuits are presented in Fig. 21(b). In order to obtain the outputs CP_1 to CP_4, the input signals V_{in} and V_{in}' having their phases shifted by a half phase from the two-phase clocks 1 and 2 is used. The operating frequency of the shift registers can be lowered to one half, as comapred with the case in which an array of shift registers is used to generate the outputs CP_1 to CP_4.

Figs. 22(a) and 22(b) are a diagram showing the structure of a circuit for generating outputs V_{01} to V_{04} having their phases shifted by one quarter by using four-phase clocks and a time chart of the circuit. In this case, the frequencies can be dropped to one quarter as low as that of an array of shift registers.

Fig. 23(a) shows a structure for generating the scanning voltages ϕ_1, ϕ_2, ϕ_3, - - -, and so on from the outputs ϕ_1, ϕ_2,- - -, and so on of a scanning voltage generator 3' by combining multi-phase clock wirings 5' and switch circuits 2'. An example of the switch circuits 2' conceivable is to generate an output voltage c from two-phase clocks a and b by two TFT elements, as shown in Fig. 23(b).

The driving waveforms are presented in Fig. 23(c). The scanning voltages ϕ_1, ϕ_2, ϕ_3 and ϕ_4 are generated by switching the output ϕ_1 with four-phase clock pulses CP_1', CP_2', CP_3' and CP_4'.

Fig. 11 shows a modification of the circuit structure of Fig. 1. In this modification, buffer circuits 19 are disposed at the output stages of the TFT elements 2 to amplify the voltages. Thus, the buffer circuits can be inserted for the purposes of the voltage amplification, level shift and so on.

Fig. 12 shows the structure in which the sampling TFTs 6 are connected with the signal input wiring and in which the scanning wirings 4 and the TFTs 2 are connected with the output stages of the TFTs 6. The operations of the circuit are similar to those of the circuit of Fig. 1. In case, however, the voltages held in the electrostatic capacitors connected with the output stages of the TFT elements 2 are influenced by the voltages applied to the gate voltages by the gate-source capacitors of the TFT elements, the clock pulses CP_1, CP_2, and CP_3 have higher frequencies than the scanning voltages ϕ_1, ϕ_2, - - -, and so on. Hence, the structure of Fig. 7 is advantageous in that it is less influenced by the gate voltages. It goes without saying that the driving methods of Figs. 4, 5 and 6 can be applied to the embodiment of Fig. 12.

Fig. 13 shows an example of the structure in case the circuit of Fig. 1 corresponds to the three color input signal wirings 1. Nine TFT elements are grouped into one block (ie. J = 1) for the video signals V_{vr}, V_{vg} and V_{vb} corresponding to the display of three colors and are sampled with the three-phase clock voltages CP_1, CP_2 and CP_3. With this structure, it is possible to drive nine pixels (corresponding to three dots, if the three colors R, G and B constitute one dot). The color arrangement of a mosaic structure can be displayed by changing the order in which the video signals V_{vr}, V_{vg} and V_{vb} are to be applied for each line.

Fig. 14 shows one example of the circuit structure using p- and n-channel CMOS switches and the driving waveforms of the circuit. In order to invert the polarities of the signals voltages for each line or frame, it is necessary to supply voltages of both positive and negative polarities. For this necessity, the switches can be constructed by the use of both p- and n-channel TFT elements to improve the operating speed.

Fig. 15 shows a method for preventing the voltages of the gates from being superposed on the sources due to the capacitive coupling by the gate-source electrostatic capacitors of the TFT elements. Each of the TFTs thus far described is replaced by two TFT elements, one of which applies the voltage of inverted logic to the gates to offset the capacitive coupling of

the gates.

Fig. 16 shows one example of forming the electrostatic capacitors acting as the capacitive loads. It is the current practice to form the electrostatic capacitors of two layers of metal electrodes and one layer of insulating film. In this example, however, a transparent electrode such as an electrode 21 is formed on a glass substrate opposed to the TFT substrate, and electrodes 20 are also formed on the portions of the TFT substrate requiring the electrostatic capacitors. Electrostatic capacitors having excellent characteristics can be formed between those two sheets of electrodes by confining a liquid crystal when the display is formed. If, in addition, those two sets of electrodes are made of transparent ones, the voltage are applied when in the circuit operations so that the liquid crystal operates to make it possible to test the operations of the circuit.

In addition to Fig. 16, in order to stabilize the circuit operations thus far described, an example, in which the transparent electrodes are removed from the opposed substrate on the circuit forming portions except the case in which the opposed glass electrodes as shown in Fig. 12 are to be used as the electrodes for forming the electrostatic capacitors, is shown in Fig. 17. A transparent electrode region 29 on an opposed glass substrate 24 is formed only on a display unit 25 but not on a scanning circuit 22 and a signal circuit 23. As a result, the circuit can be speeded up by reducing the electrostatic capacitive coupling between the individual portions of the circuit and the opposed glass substrate.

Fig. 24 shows a modification of the circuit of Fig. 1. A plurality of TFT elements 101 are arrayed such that a k-number of TFT elements have their drain electrodes connected with a k-number of data electrodes 102, respectively, and their gate electrodes connected with one block scanning electrode 103. Output electrodes 104 connected with the source electrodes of the k-number of TFT elements are connected with buffer circuits or voltage converters 107 to output voltages at signal electrodes 108 of a display unit. In the present embodiment, the data electrodes 102 are arranged at the input side of the TFT elements 101 but do not intersect the output electrodes 104. Moreover, the buffer circuits 107 are formed between the output electrodes 104 and the display unit, and a scanning electrode 109 of the display unit and the output electrodes 104 do not intersect. With this structure, it is possible to avoid the voltages, which have their levels always varying with time like the data signal voltages or the scanning voltage of the display unit with respect to the output electrodes 104 of the TFT elements 101, from being superposed as noises on the signal voltages by the electrostatic capacitive coupling. Even if the TFT elements 101 are constructed to have a small shape, moreover, the S/N ratio of the signal voltages can be increased.

In addition to the structure thus far described, a capacitive electrode 105 can be made to intersect the output electrodes 104 while interposing an insulating film to form a built-in capacitor 106, thereby increasing the stability of the output voltages applied by the TFTs 101.

The buffer circuits 107 may be the so-called "multiplexer circuit" for selecting the output voltages from voltages at a plurality of levels, or a circuit having a high impedance at its input side and a low impedance at its output side, such as an analog voltage amplifier.

According to the embodiment of Fig. 24, the fluctuations of the waveforms due to the capacitive coupling to other wirings can be reduced at the output portion of the divided matrix circuit so that a stable output voltage can be obtained to improve the display characteristics of the display unit. Thanks to the small fluctuations of the waveforms due to the capacitive coupling to the output portion, moreover, the capacities to be established at the output portion can be dropped to a small value, and the TFT elements of the driving divided matrix circuit can be made small while improving the operating speed of the divided matrix circuit.

Incidentally, the embodiments thus far described are exemplified by the sequential line scanning method. Despite of this fact, however, naturally the present invention can be applied to the sequential dot scanning method.

Claims

1. A method of scanning an array;

the array comprising:

K ($K \geqq 3$) consecutive semiconductor switch elements (6) connected to at least one further switch element (2), each of said consecutive switch elements having a first main electrode connected to said at least one further switch element (2), a second main electrode, and a control electrode responsive to a control signal (CP_1, CP_2, CP_3) for controlling the transmissive and intransmissive states between the first and second main electrodes;

said at least one further switch element (2) being responsive to at least one further control signal (ϕ_1, ϕ_2, ϕ_3) for controlling the transmissive and intransmissive states of said at least one further switch element between at least one input signal (V_v, V_{vr}, V_{vg}, V_{vb}) and the consecutive switch elements (6); and

capacitive loads (7) connected respectively to the second main electrodes of each of said consecutive semiconductor switch elements (6);

the method comprising:

repeatedly scanning the array with a predetermined scanning period, the scanning of the

array including causing each of the K consecutive semiconductor switch elements (6) to have at least one transmissive period and at least one intransmissive period, during which transmissive period the at least one input signal is applied to the corresponding capacitive load;

characterised in that:

the time for which a selected number L (K > L ≧ 2) of adjacent ones of the consecutive semiconductor switch elements (6) are all rendered transmissive and the time for which said selected number of semiconductor switch elements are all rendered intransmissive are included in a period which is less than said predetermined scanning period, and that the total duration of one transmissive period and one intransmissive period of any one of the K consecutive semiconductor switch elements (6) is also less than said predetermined scanning period.

2. A method according to claim 1, wherein the or each further switch element (2) is connected to a plurality of said consecutive switch elements (6).

3. A method according to claim 1, wherein there are a plurality of said further switch elements, each of said further switch elements is connected to a corresponding one of the consecutive switch elements, there are a plurality of input signals, and each of said further switch elements connecting a respective one of said input signals to the corresponding one of the consecutive switch elements.

4. A method of scanning an array;

the array comprising:

K (K ≧ 3) consecutive semiconductor switch elements (101, 102, 103, 104) each having a first main electrode responsive to an input signal (V_{in}), a second main electrode, and a control electrode responsive to a control signal (ϕ_1, ϕ_2, ϕ_3, ϕ_4) for controlling the transmissive and intransmissive states of the input signal (V_{in}) between the first and second main electrodes; and

capacitive loads (201, 202, 203, 204) connected respectively to the second main electrodes of each of said consecutive semiconductor switch elements (101, 102, 103, 104);

the method comprising:

repeatedly scanning the array with a predetermined scanning period, the scanning of the array including causing each of the K consecutive semiconductor switch elements (101, 102, 103, 104) to have at least one transmissive period and at least one intransmissive period, during which transmissive period the input signal is applied to the corresponding capacitive load;

characterised in that:

the time for which a selected number L (K > L ≧ 2) of adjacent ones of the consecutive semiconductor switch elements (101, 102, 103, 104) are all rendered transmissive and the time for which said selected number L of semiconductor switch elements are all rendered intransmissive are included in a period which is less than said predetermined scanning period, and that the total duration of one transmissive period and one intransmissive period of any one of the K consecutive semiconductor switch elements (6) is also less than said predetermined scanning period.

5. A scanning method according to any one of the preceding claims wherein;

the semiconductor switch elements (2,6) are arranged in the array in J (J ≧ 1) blocks, each block including M (M ≧ 3; K = J x M) semiconductor switch elements (2,6); and

L is selected so as to be in the vicinity of M/2.

6. A scanning method according to claim 5, wherein M is such that M = 2L - 1, M = 2L or M = 2L + 1.

7. A scanning circuit having:

an array comprising:

K (K ≧ 3) consecutive semiconductor switch elements (6) connected to at least one further switch element (2), each of said consecutive switch elements having a first main electrode connected to said at least one further switch element (2), a second main electrode, and a control electrode responsive to a control signal (CP_1, CP_2, CP_3) for controlling the transmissive and intransmissive states between the first and second main electrodes;

capacitive loads connected respectively to the second main electrodes of each semiconductor switch elements (6);

said at least one further switch element (2) being responsive to at least one further control signal (ϕ_1, ϕ_2, ϕ_3) for controlling the transmissive and intransmissive states of said at least one further switch element between at least one input signal (V_v, V_{vr}, V_{vg}, V_{vb}) and the consecutive switch elements (6);

an input signal source (1) for generating said at least one input signal (V_v, V_{vr}, V_{vg}, V_{vb}) for said further semiconductor switch elements (6); and

a control circuit (3,13) for generating said control signal of said semiconductor switch elements (2, 6), said control circuit (3,13) being arranged to generate said control signals sequentially so as repeatedly to scan the array with a predetermined scanning period, the scanning of the array including causing each of the K semicon-

ductor switch elements (6) to have at least one transmissive period and at least one intransmissive period, during which transmissive period the input signal is applied to the corresponding capacitive load;

characterised in that:

the control circuit (3,13) is arranged such that the time for which a selected number L (K > L ≧ 2) of adjacent ones of the consecutive semiconductor switch elements are all rendered transmissive and the time for which said selected number of semiconductor switch elements are all rendered intransmissive are included in a period which is less than said predetermined scanning period, and that the total duration of one transmissive period and one intransmissive period of any one of the K consecutive semiconductor switch elements (6) is also less than said predetermined scanning period.

8. A scanning circuit according to claim 7, wherein the or each further switch element (2) is connected to a plurality of said consecutive switch elements (6).

9. A scanning circuit according to claim 7, wherein there are a plurality of said further switch elements, each of said further switch elements is connected to a corresponding one of the consecutive switch elements, there are a plurality of input signals, and each of said further switch elements connecting a respective one of said input signals to the corresponding one of the consecutive switch elements.

10. A scanning circuit having:

an array comprising:

K (K ≧ 3) consecutive semiconductor switch elements (101, 102, 103, 104) each having a first main electrode responsive to an input signal (V_{in}), a second main electrode, and a control electrode responsive to a control signal (ϕ_1, ϕ_2, ϕ_3, ϕ_4) for controlling the transmissive and intransmissive states of the input signal (V_{in}) between the first and second main electrodes;

capacitive loads (201, 202, 203, 204) connected respectively to the second main electrodes of each of said consecutive semiconductor switch elements (101, 102, 103, 104):

an input signal source (1) for generating said input signals (V_{in}) of said semiconductor switch elements (6); and

a control circuit (3,13) for generating said control signals of said semiconductor switch elements (2, 6), said control circuit (3,13) being arranged to generate said control signals sequentially so as repeatedly to scan the array with a predetermined scanning period, the scanning of the array including causing each of the K semiconductor switch elements (6) to have at least one transmissive period and at least one intransmissive period, during which transmissive period the input signal is applied to the corresponding capacitive load;

characterised in that:

the control circuit (3,13) is arranged such that

the time for which a selected number L (K > L ≧ 2) of adjacent ones of the consecutive semiconductor switch elements are all rendered transmissive and the time for which said selected number of semiconductor switch elements are all rendered intransmissive are included in a period which is less than said predetermined scanning period, and that the total duration of one transmissive period and one intransmissive period of any one of the K consecutive semiconductor switch elements (6) is also less than said predetermined scanning period;

11. A scanning circuit according to any one of claims 7 to 14, wherein the semiconductor switch elements (2,6) are arranged in the array in J (J ≧ 1) blocks, each block including M (M ≧ 3; K = J x M) semiconductor switch elements (2,6);

12. A scanning circuit according to claim 11 wherein L is in the vicinity of M/2.

13. A scanning circuit according to claim 12 wherein M is such that M = 2L - 1, M = 2L or M = 2L + 1.

14. A scanning circuit according to any one of claims 7 to 13 wherein said semiconductor switch elements and said capacitive loads are formed on a common substrate.

Patentansprüche

1. Verfahren zum Durchrastern eines Arrays,
   - wobei das Array folgendes aufweist:
     -- K (K ≧ 3) aufeinanderfolgende Halbleiter-Schaltelemente (6), die mit mindestens einem weiteren Schaltelement (2) verbunden sind, wobei jedes der aufeinanderfolgenden Schaltelemente eine erste, mit dem mindestens einen weiteren Schaltelement (2) verbundene Hauptelektrode, eine zweite Hauptelektrode und eine Steuerelektrode aufweist, die auf ein Steuersignal (CP_1, CP_2, CP_3) anspricht, um einen durchlässigen und einen sperrenden Zustand zwischen der ersten und der zweiten Hauptelektrode zu steuern;

-- wobei das mindestens eine weitere Schaltelement (2) auf mindestens ein weiteres Steuersignal (Φ_1, Φ_2, Φ_3) reagiert, um den durchlassenden und den sperrenden Zustand des mindestens einen weiteren Schaltelements zwischen mindestens einem Eingangssignal (V_v, V_{vr}, V_{vg}, V_{vb}) und den aufeinanderfolgenden Schaltelementen (6) zu steuern; und

-- kapazitiven Lasten (7), die jeweils an die zweiten Hauptelektroden jedes der aufeinanderfolgenden Halbleiter-Schaltelemente (6) angeschlossen sind;

- wobei das Verfahren folgendes aufweist:

-- wiederholtes Durchrastern des Arrays mit einer vorgegebenen Durchrasterperiode, wobei es zum Durchrastern des Arrays gehört, daß bewirkt wird, daß jedes der K aufeinanderfolgenden Halbleiter-Schaltelemente (6) mindestens eine durchlassende Periode und mindestens eine sperrende Periode aufweist, wobei während der durchlassenden Periode das mindestens eine Eingangssignal an die zugehörige kapazitive Last angelegt wird;

dadurch gekennzeichnet, daß:

- die Zeit, in der eine ausgewählte Anzahl L ($K > L \geq 2$) benachbarter aufeinanderfolgender Halbleiter-Schaltelemente (6) alle leitend gemacht sind, und die Zeit, in der diese ausgewählte Anzahl von Halbleiter-Schaltelementen alle sperrend gemacht sind, in einer Periode enthalten sind, die kürzer als die vorgegebene Durchrasterperiode ist, und daß die Gesamtdauer einer Durchlaßperiode und einer Sperrperiode jedes der K aufeinanderfolgenden Halbleiter-Schaltelemente (6) ebenfalls kleiner als die vorgegebene Durchrasterperiode ist.

2. Verfahren nach Anspruch 1, bei dem das oder jedes weitere Schaltelement (2) mit mehreren der aufeinanderfolgenden Schaltelemente (6) verbunden ist.

3. Verfahren nach Anspruch 1, bei dem mehrere weitere Schaltelemente vorliegen, wobei jedes der weiteren Schaltelemente mit einem entsprechenden der aufeinanderfolgenden Schaltelemente verbunden ist, mehrere Eingangssignale vorhanden sind und jedes der weiteren Schaltelemente ein jeweiliges der Eingangssignale mit dem entsprechenden der aufeinanderfolgenden Schaltelemente verbindet.

4. Verfahren zum Durchrastern eines Arrays,

- wobei das Array folgendes aufweist:

-- K ($K \geq 3$) aufeinanderfolgende Halbleiter-Schaltelemente (101, 102, 103, 104), von denen jedes eine erste, auf ein Eingangssignal (V_{In}) ansprechende Hauptelektrode, eine zweite Hauptelektrode und eine Steuerelektrode aufweist, die auf ein Steuersignal (Φ_1, Φ_2, Φ_3, Φ_4) anspricht, um einen durchlässigen und einen sperrenden Zustand für das Eingangssignal (V_{In}) zwischen der ersten und der zweiten Hauptelektrode zu steuern;

-- kapazitiven Lasten (201, 202, 203, 204), die jeweils an die zweiten Hauptelektroden jedes der aufeinanderfolgenden Halbleiter-Schaltelemente (101, 102, 103, 104) angeschlossen sind;

- wobei das Verfahren folgendes aufweist:

-- wiederholtes Durchrastern des Arrays mit einer vorgegebenen Durchrasterperiode, wobei es zum Durchrastern des Arrays gehört, daß bewirkt wird, daß jedes der K aufeinanderfolgenden Halbleiter-Schaltelemente (101, 102, 103, 104) mindestens eine durchlassende Periode und mindestens eine sperrende Periode aufweist, wobei während der durchlassenden Periode das eine Eingangssignal an die zugehörige kapazitive Last angelegt wird;

dadurch gekennzeichnet, daß:

- die Zeit, in der eine ausgewählte Anzahl L ($K > L \geq 2$) benachbarter aufeinanderfolgender Halbleiter-Schaltelemente (101, 102, 103, 104) alle leitend gemacht sind, und die Zeit, in der diese ausgewählte Anzahl L von Halbleiter-Schaltelementen alle sperrend gemacht sind, in einer Periode enthalten sind, die kürzer als die vorgegebene Durchrasterperiode ist, und daß die Gesamtdauer einer Durchlaßperiode und einer Sperrperiode jedes der K aufeinanderfolgenden Halbleiter-Schaltelemente (6) ebenfalls kleiner als die vorgegebene Durchrasterperiode ist.

5. Durchrasterungsverfahren nach einem der vorstehenden Ansprüche, bei dem:

- die Halbleiter-Schaltelemente (2, 6) im Array in J ($J \geq 1$) Blöcken angeordnet sind, von denen jeder M ($M \geq 3$; $K = J \times M$) Halbleiter-Schaltelemente (2, 6) enthält; und
- L so ausgewählt ist, daß es in der Nähe von M/2 liegt.

6. Durchrasterungsverfahren nach Anspruch 5, bei dem M dergestalt ist, daß $M = 2L - 1$, $M = 2L$ oder $M = 2L + 1$ gilt.

7. Durchrasterschaltung mit einem Array mit:
   -- K ($K \geqq 3$) aufeinanderfolgende Halbleiter-Schaltelemente (6), die mit mindestens einem weiteren Schaltelement (2) verbunden sind, wobei jedes der aufeinanderfolgenden Schaltelemente eine erste, mit dem mindestens einen weiteren Schaltelement (2) verbundene Hauptelektrode, eine zweite Hauptelektrode und eine Steuerelektrode aufweist, die auf ein Steuersignal (CP_1, CP_2, CP_3) anspricht, um einen durchlässigen und einen sperrenden Zustand zwischen der ersten und der zweiten Hauptelektrode zu steuern;
   -- kapazitiven Lasten, die jeweils an die zweiten Hauptelektroden jedes der aufeinanderfolgenden Halbleiter-Schaltelemente (6) angeschlossen sind;
   - wobei das mindestens eine weitere Schaltelement (2) auf mindestens ein weiteres Steuersignal (Φ_1, Φ_2, Φ_3) reagiert, um den durchlassenden und den sperrenden Zustand des mindestens einen weiteren Schaltelements zwischen mindestens einem Eingangssignal (V_v, V_{vr}, V_{vg}, V_{vb}) und den aufeinanderfolgenden Schaltelementen (6) zu steuern;
   - einer Eingangssignalquelle (1) zum Erzeugen des mindestens einen Eingangssignals (V_v, V_{vr}, V_{vg}, V_{vb}) für die weiteren Halbleiter-Schaltelemente (6); und
   - einer Steuerschaltung (3, 13) zum Erzeugen des Steuersignals für die Halbleiter-Schaltelemente (2, 6), die so ausgebildet ist, daß sie die Steuersignale sequentiell erzeugt, um das Array wiederholt mit einer vorgegebenen Durchrasterperiode durchzurastern, wobei es zum Durchrastern des Arrays gehört, daß bewirkt wird, daß jedes der K Halbleiter-Schaltelemente (6) mindestens eine durchlassende Periode und mindestens eine sperrende Periode aufweist, wobei während der durchlassenden Periode das Eingangssignal an die entsprechende kapazitive Last gelegt wird;
   dadurch gekennzeichnet, daß
   - die Steuerschaltung (3, 13) so ausgebildet ist, daß die-Zeit, in der eine ausgewählte Anzahl L ($K > L \geqq 2$) benachbarter aufeinanderfolgender Halbleiter-Schaltelemente alle leitend gemacht sind, und die Zeit, in der diese ausgewählte Anzahl von Halbleiter-Schaltelementen alle sperrend gemacht sind, in einer Periode enthalten sind, die kürzer als die vorgegebene Durchrasterperiode ist, und daß die Gesamtdauer einer Durchlaßperiode und einer Sperrperiode jedes der K aufeinanderfolgenden Halbleiter-Schaltelemente (6) ebenfalls kleiner als die vorgegebene Durchrasterperiode ist.

8. Durchrasterschaltung nach Anspruch 7, bei der das oder jedes weitere Schaltelement (2) mit mehreren der aufeinanderfolgenden Schaltelemente (6) verbunden ist.

9. Durchrasterschaltung nach Anspruch 7, bei der mehrere weitere Schaltelemente vorliegen, wobei jedes der weiteren Schaltelemente mit einem entsprechenden der aufeinanderfolgenden Schaltelemente verbunden ist, mehrere Eingangssignale vorhanden sind und jedes der weiteren Schaltelemente ein jeweiliges der Eingangssignale mit dem entsprechenden der aufeinanderfolgenden Schaltelemente verbindet.

10. Durchrasterschaltung mit einem Array mit:
   -- K ($K \geqq 3$) aufeinanderfolgende Halbleiter-Schaltelemente (101, 102, 103, 104), von denen jedes eine erste, auf ein Eingangssignal (V_{in}) ansprechende Hauptelektrode, eine zweite Hauptelektrode und eine Steuerelektrode aufweist, die auf ein Steuersignal (Φ_1, Φ_2, Φ_3, Φ_4) anspricht, um einen durchlässigen und einen sperrenden Zustand für das Eingangssignal (V_{in}) zwischen der ersten und der zweiten Hauptelektrode zu steuern;
   -- kapazitiven Lasten (201, 202, 203, 204), die jeweils an die zweiten Hauptelektroden jedes der aufeinanderfolgenden Halbleiter-Schaltelemente (101, 102, 103, 104) angeschlossen sind;
   - einer Eingangssignalquelle (1) zum Erzeugen der Eingangssignale (V_{in}) für die Halbleiter-Schaltelemente (6); und
   - einer Steuerschaltung (3, 13) zum Erzeugen der Steuersignale für die Halbleiter-Schaltelemente (2, 6), die so ausgebildet sind, daß sie die Steuersignale sequentiell erzeugen, um das Array wiederholt mit einer vorgegebenen Durchrasterperiode durchzurastern, wobei es zum Durchrastern des Arrays gehört, daß bewirkt wird, daß jedes der K Halbleiter-Schaltelemente (6) mindestens eine durchlassende Periode und mindestens eine sperrende Periode aufweist, wobei während derdurchlassenden Periode das Eingangssignal an die entsprechende kapazitive Last gelegt wird;
   dadurch gekennzeichnet, daß
   - die Steuerschaltung (3, 13) so ausgebildet ist, daß die-Zeit, in der eine ausgewählte Anzahl L ($K > L \geqq 2$) benachbarter aufeinanderfolgender Halbleiter-Schaltelemente alle leitend gemacht sind, und die Zeit, in

der diese ausgewählte Anzahl von Halbleiter-Schaltelementen alle sperrend gemacht sind, in einer Periode enthalten sind, die kürzer als die vorgegebene Durchrasterperiode ist, und daß die Gesamtdauer einer Durchlaßperiode und einer Sperrperiode jedes der K aufeinanderfolgenden Halbleiter-Schaltelemente (6) ebenfalls kleiner als die vorgegebene Durchrasterperiode ist.

11. Durchrasterschaltung nach einem der Ansprüche 7 bis 14, bei der die Halbleiter-Schaltelemente (2, 6) im Array in J (J ≧ 1) Blöcken angeordnet sind, von denen jeder M (M ≧ 3; K = J x M) Halbleiter-Schaltelemente (2, 6) enthält.

12. Durchrasterschaltung nach Anspruch 11, bei der L in der Nähe von M/2 liegt.

13. Durchrasterschaltung nach Anspruch 12, bei der M dergestalt ist, daß M = 2L - 1, M = 2L oder M = 2L + 1 gilt.

14. Durchrasterschaltung nach einem der Ansprüche 7 bis 13, bei der die Halbleiter-Schaltelemente und die kapazitiven Lasten auf einem gemeinsamen Substrat ausgebildet sind.

Revendications

1. Procédé d'exploration d'un réseau par balayage, le réseau comprenant :

K (K = 3) éléments de commutation à semiconducteurs successifs (6) raccordés à au moins un autre élément de commutation (2), chacun desdits éléments de commutation successifs possédant une première électrode principale raccordée audit au moins un autre élément de commutation (2), une seconde électrode principale, et une électrode de commande apte à répondre à un signal de commande (CP1, CP2, CP3) pour la commande des états passant et bloqué entre les première et seconde électrodes principales;

ledit au moins un autre élément de commutation (2) étant apte à répondre à au moins un autre signal de commande (f1, f2, f3) pour la commande des états passant et bloqué dudit au moins un autre élément de commutation entre au moins un signal d'entrée (Vv, Vvr, Vvg, Vvb) et les éléments de commutation successifs (6); et

des charges capacitives (7) raccordées respectivement aux secondes électrodes principales de chacun desdits éléments de commutation à semiconducteurs successifs (6);

le procédé consistant à :

explorer par balayage de façon répétée le réseau avec une période de balayage prédéterminée, l'exploration par balayage du réseau consistant à amener chacun des K éléments de commutation à semiconducteurs successifs (6) à posséder au moins une période de transmission et au moins une période de blocage, le au moins un signal d'entrée étant appliqué, pendant la période de blocage, à la charge capacitive correspondante;

caractérisé en ce que :

la durée, pendant laquelle un nombre sélectionné L (K > L = 2) d'éléments de commutation adjacents faisant partie des éléments de commutation à semiconducteurs successifs (6) sont tous rendus passants, et la durée, pendant laquelle ledit nombre sélectionné d'éléments de commutation à semiconducteurs sont tous placés à l'état bloqué, sont incluses dans une période qui est inférieure à ladite période de balayage prédéterminée, et que la durée totale d'une période de transmission et d'une période de blocage de l'un quelconque des K éléments de commutation à semiconducteurs successifs (6) est également inférieure à ladite période de balayage prédéterminée.

2. Procédé selon la revendication 1, dans lequel le ou chaque autre élément de commutation (2) est raccordé à une pluralité desdits éléments de commutation successifs (6).

3. Procédé selon la revendication 1, dans lequel il est prévu une pluralité desdits autres éléments de commutation, chacun desdits autres éléments de commutation est raccordé à l'un correspondant des éléments de commutation successifs, il est prévu une pluralité de signaux d'entrée, et chacun desdits autres éléments de commutation raccorde l'un respectif desdits signaux d'entrée à l'un correspondant des éléments de commutation successifs.

4. Procédé d'exploration d'un réseau par balayage;

le réseau comprenant

K (K = 3) éléments de commutation à semiconducteurs successifs (101,102,103,104) possédant chacun une première électrode principale apte à répondre à un signal d'entrée (Vin), une seconde électrode principale et une électrode de commande apte à répondre à un signal de commande (f1, f2, f3, f4) pour la commande de l'état passant et de l'état bloqué pour le signal d'entrée (Vin) entre les première et seconde électrodes principales;

des charges capacitives (201, 202, 203, 204) raccordées respectivement aux secondes électrodes principales de chacun desdits élé-

ments de commutation à semiconducteurs successifs (101, 102, 103, 104);

le procédé consistant à :

explorer par balayage de façon répétée le réseau avec une période de balayage prédéterminée, l'exploration du réseau par balayage consistant à amener chacun des K éléments de commutation à semiconducteurs successifs (101, 102, 103, 104) à posséder au moins une période de transmission et au moins une période de blocage, le signal d'entrée étant appliqué à la charge capacitive correspondante, pendant la période de transmission;

caractérisé en ce que :

la durée pendant laquelle un nombre sélectionné L (K > L = 2) d'éléments de commutation adjacents faisant partie des éléments de commutation à semiconducteurs successifs (101,102,103,104) sont tous rendus conducteurs et la durée, pendant laquelle ledit nombre sélectionné L d'éléments de commutation à semiconducteurs sont tous placés à l'état bloqué, sont incluses dans une période qui est inférieure à ladite période de balayage prédéterminée, et que la durée totale d'une période de transmission et d'une période de blocage de l'un quelconque des K éléments de commutation à semiconducteurs successifs (6) est également inférieure à ladite période de balayage prédéterminée.

5. Procédé d'exploration par balayage selon l'une quelconque des revendications précédentes, dans lequel :

les éléments de commutation à semiconducteurs (2,6) sont disposés dans le réseau suivant J (J = 1) blocs, chaque bloc contenant M (M = 3; K = J x M) éléments de commutation à semiconducteurs (2,6); et

L est choisi de manière à être voisin de M/2.

6. Procédé d'exploration par balayage selon la revendication 5, dans lequel M est tel que M = 2L - 1, M = 2L ou M = 2L +1.

7. Circuit d'exploration par balayage comportant :

un réseau comprenant :

K (K = 3) éléments de commutation à semiconducteurs successifs (6) raccordés à au moins un autre élément de commutation (2), chacun desdits éléments de commutation successifs possédant une première électrode principale raccordée audit au moins un autre élément de commutation (2), une seconde électrode principale, et une électrode de commande apte à répondre à un signal de commande (CP1, CP2, CP3) pour la commande des états passant et bloqué entre les première et seconde électrodes principales;

des charges capacitives raccordées respectivement aux secondes électrodes principales de chacun desdits éléments de commutation à semiconducteurs (6);

ledit au moins un autre élément de commutation (2) étant apte à répondre à au moins un autre signal de commande (f1, f2, f3) pour la commande des états passant et bloqué dudit au moins un autre élément de commutation entre au moins un signal d'entrée (Vv, Vvr, Vvg, Vvb) et les éléments de commutation successifs (6);

une source de signaux d'entrée (1) servant à produire ledit au moins un signal d'entrée (Vv, Vvr, Vvg, Vvb) pour lesdits autres éléments de commutation à semiconducteurs (6); et

un circuit de commande (3,13) servant à produire ledit signal de commande desdits éléments de commutation à semiconducteurs (2,6), ledit circuit de commande (3,13) étant agencé de manière à produire lesdits signaux de commande séquentiellement de manière à explorer par balayage de façon répétée le réseau avec une période de balayage prédéterminée, l'exploration du réseau par balayage consistant à amener chacun des K éléments de commutation à semiconducteurs (6) à posséder au moins une période de transmission et au moins une période de blocage, le signal d'entrée étant appliqué à la charge capacitive correspondante pendant la période de transmission;

caractérisé en ce que :

le circuit de commande (3,13) est agencé de telle sorte que la durée, pendant laquelle un nombre sélectionné L (K > L = 2) d'éléments de commutation adjacents faisant partie des éléments de commutation à semiconducteurs successifs sont tous rendus passants et la durée, pendant laquelle ledit nombre sélectionné d'éléments de commutation à semiconducteurs sont tous placés à l'état bloqué, sont incluses dans une période qui est inférieure à ladite période de balayage prédéterminée, et que la durée totale d'une période de transmission et d'une période de blocage de l'un quelconque des K éléments de commutation à semiconducteurs successifs (6) est également inférieure à ladite période de balayage prédéterminée.

8. Circuit d'exploration par balayage selon la revendication 7, dans lequel le ou chaque autre élément de commutation (2) est connecté à une pluralité desdits éléments de commutation successifs (6).

9. Circuit d'exploration par balayage selon la revendication 7, dans lequel il est prévu une pluralité

desdits autres éléments de commutation, chacun desdits autres éléments de commutation est raccordé à l'un correspondant des éléments de commutation successifs, il est prévu une pluralité de signaux d'entrée, et chacun desdits autres éléments de commutation raccordant l'un respectif desdits signaux d'entrée à l'un correspondant des éléments de commutation successifs.

10. Circuit d'exploration par balayage comportant :

un réseau comprenant :

K (K = 3) éléments de commutation à semiconducteurs successifs (101,102,103,104) possédant chacun une première électrode principale apte à répondre à un signal d'entrée (Vin), une seconde électrode principale et une électrode de commande apte à répondre à un signal de commande (f1, f2, f3, f4) pour la commande de l'état passant et de l'état bloqué pour le signal d'entrée (Vin) entre les première et seconde électrodes principales;

des charges capacitives (201, 202, 203, 204) raccordées respectivement aux secondes électrodes principales de chacun desdits éléments de commutation à semiconducteurs successifs (101, 102, 103, 104);

une source de signaux d'entrée (1) servant à produire lesdits signaux d'entrée (Vin) desdits éléments de commutation à semiconducteurs (6); et

un circuit de commande (3,13) servant à produire lesdits signaux de commande desdits éléments de commutation à semiconducteurs (2,6), ledit circuit de commande (3,13) étant agencé de manière à produire lesdits signaux de commande séquentiellement de manière à explorer par balayage de façon répétée le réseau avec une période de balayage prédéterminée, l'exploration du réseau par balayage consistant à amener chacun des K éléments de commutation à semiconducteurs (6) à posséder au moins une période de transmission et au moins une période de blocage, le signal d'entrée étant appliqué à la charge capacitive correspondante pendant la période de transmission;

caractérisé en ce que :

le circuit de commande (3,13) est agencé de telle sorte que la durée, pendant laquelle un nombre sélectionné L (K > L = 2) d'éléments de commutation adjacents faisant partie des éléments de commutation à semiconducteurs successifs sont tous rendus passants et la durée, pendant laquelle ledit nombre sélectionné d'éléments de commutation à semiconducteurs sont tous placés à l'état bloqué, sont incluses dans une période qui est inférieure à ladite période de balayage prédéterminée, et que la durée totale d'une période de transmission et d'une période de blocage de l'un quelconque des K éléments de commutation à semiconducteurs successifs (6) est également inférieure à ladite période de balayage prédéterminée.

11. Circuit d'exploration par balayage selon l'une quelconque des revendications 7 à 14, dans lequel les éléments de commutation à semiconducteurs (2,6) sont disposés dans le réseau suivant J (J = 1) blocs, chaque bloc contenant M (M = 3; K = J x M) éléments de commutation à semiconducteurs (2,6).

12. Circuit d'exploration par balayage selon la revendication 11, dans lequel L est voisin de M/2.

13. Circuit d'exploration par balayage selon la revendication 12, dans lequel M est tel que M = 2L - 1, M = 2L ou M = 2L + 1.

14. Circuit d'exploration par balayage selon l'une quelconque des revendications 7 à 13, dans lequel lesdits éléments de commutation à semiconducteurs et lesdites charges capacitives sont formés sur un substrat commun.

FIG. 1

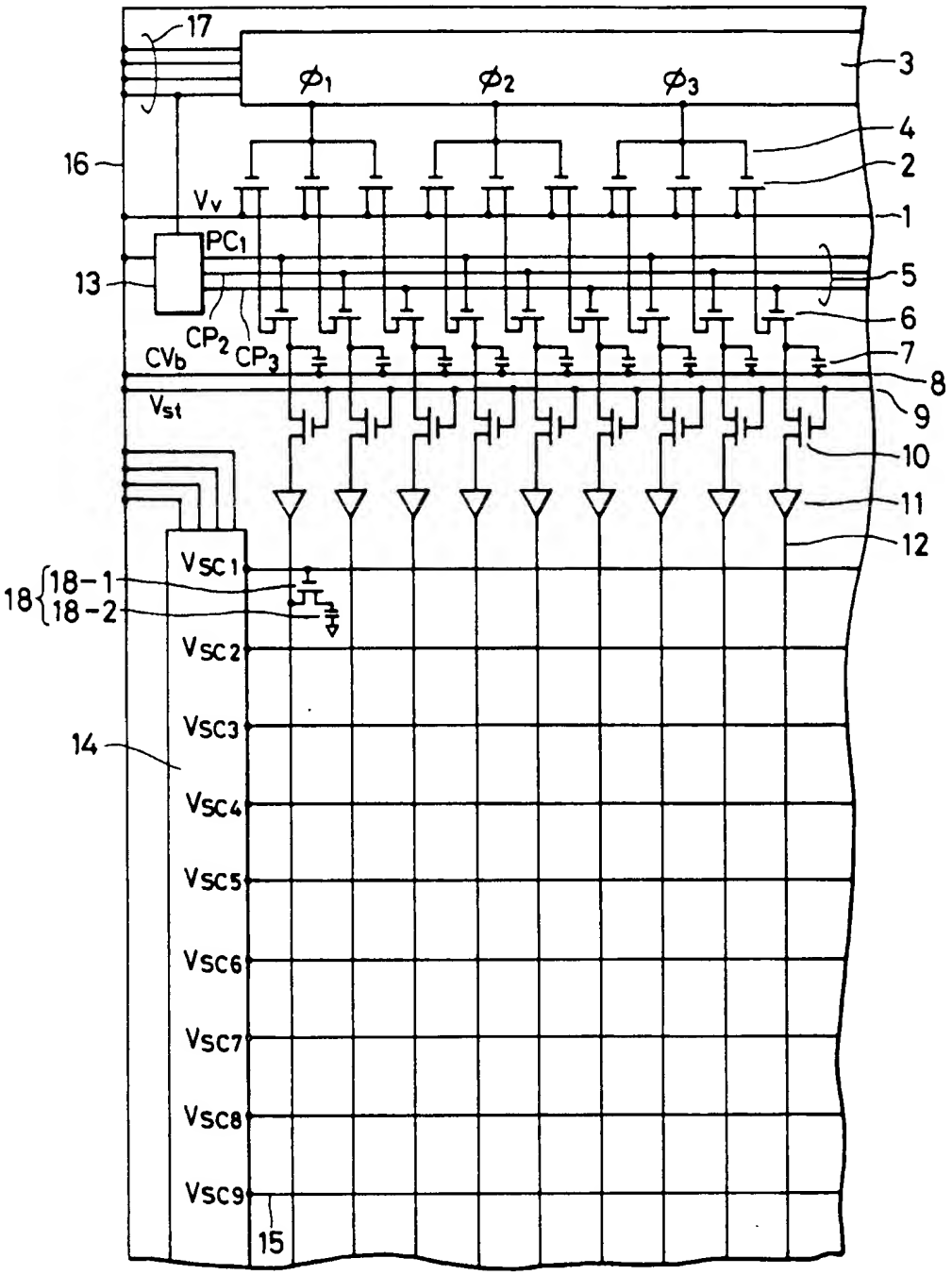

17
3
ϕ_1
ϕ_2
ϕ_3
4
16
2
V_v
1
PC_1
13
5
CP_2
CP_3
6
CV_b
7
8
V_{st}
9
10
11
12
18
18-1
18-2
V_{SC1}
V_{SC2}
V_{SC3}
14
V_{SC4}
V_{SC5}
V_{SC6}
V_{SC7}
V_{SC8}
V_{SC9}
15

FIG. 2

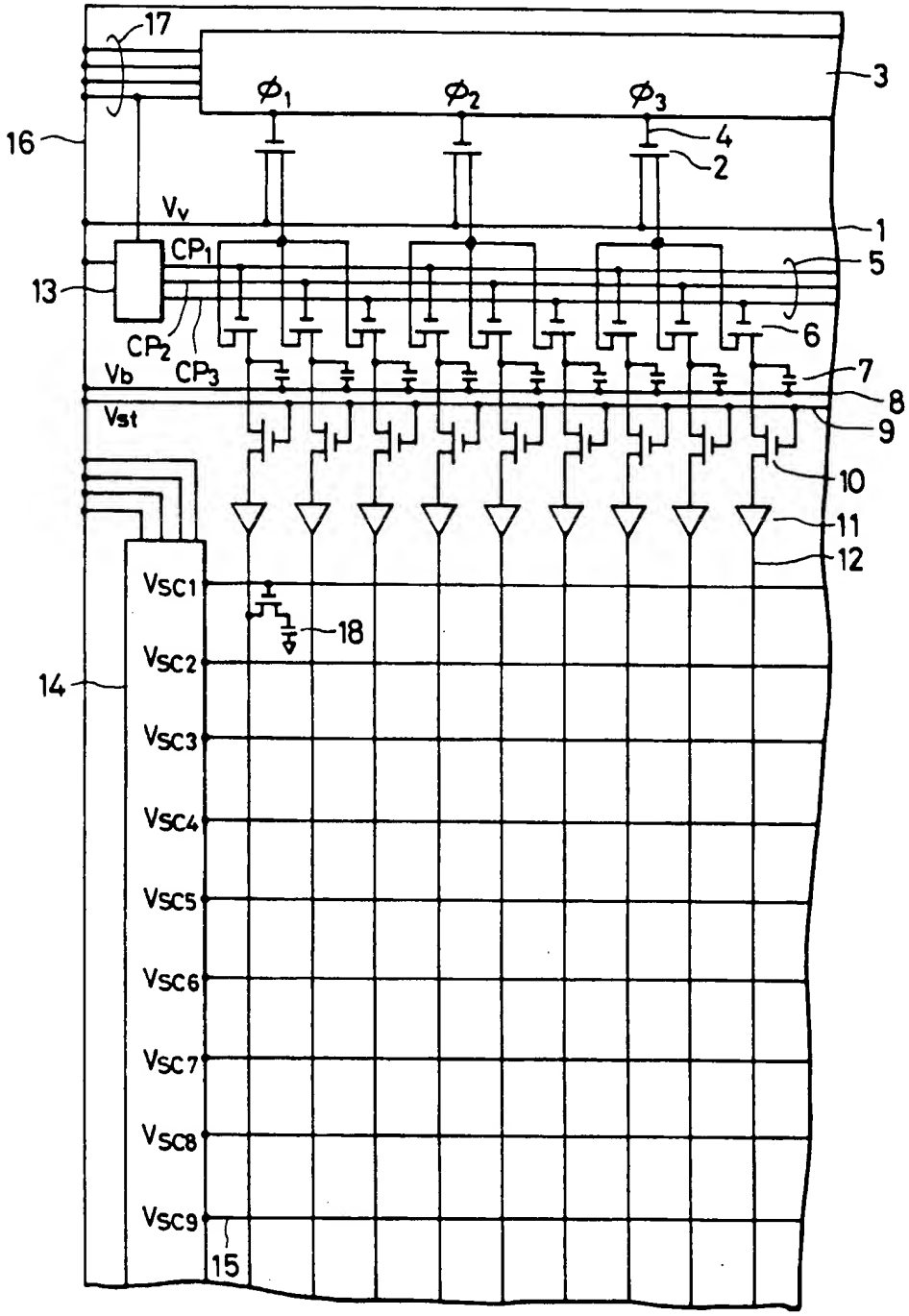

17
3
ϕ_1
ϕ_2
ϕ_3
16
4
2
V_v
1
CP_1
5
13
CP_2
CP_3
6
Vb
7
8
Vst
9
10
11
12
Vsc1
18
Vsc2
14
Vsc3
Vsc4
Vsc5
Vsc6
Vsc7
Vsc8
Vsc9
15

FIG. 3

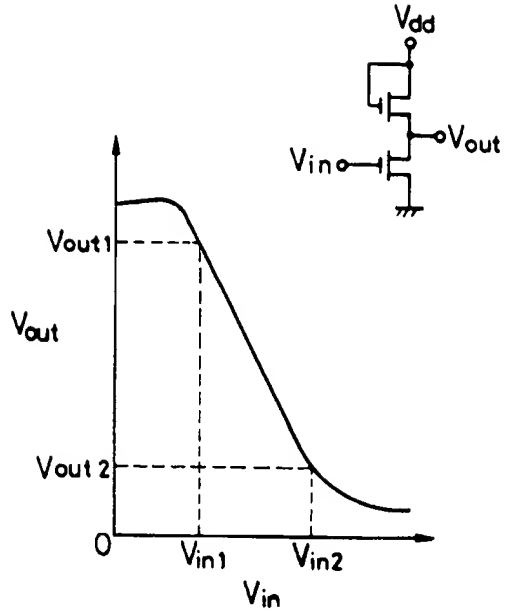

Vdd
Vout
Vin
Vout1
Vout
Vout2
0
Vin1
Vin2
Vin

FIG. 4

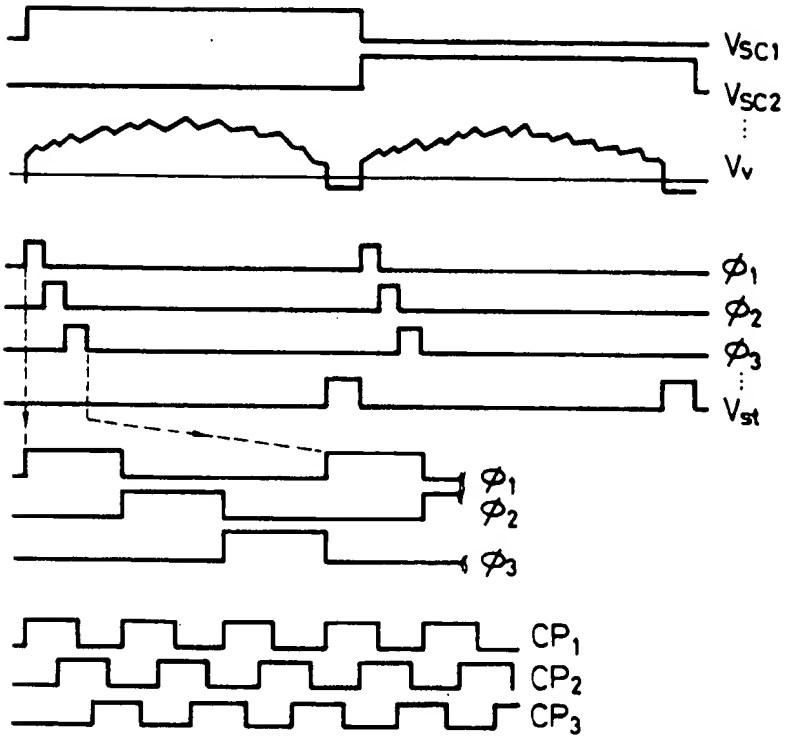

Vsc1
Vsc2
Vv
φ1
φ2
φ3
Vst
φ1
φ2
φ3
CP1
CP2
CP3

FIG. 5

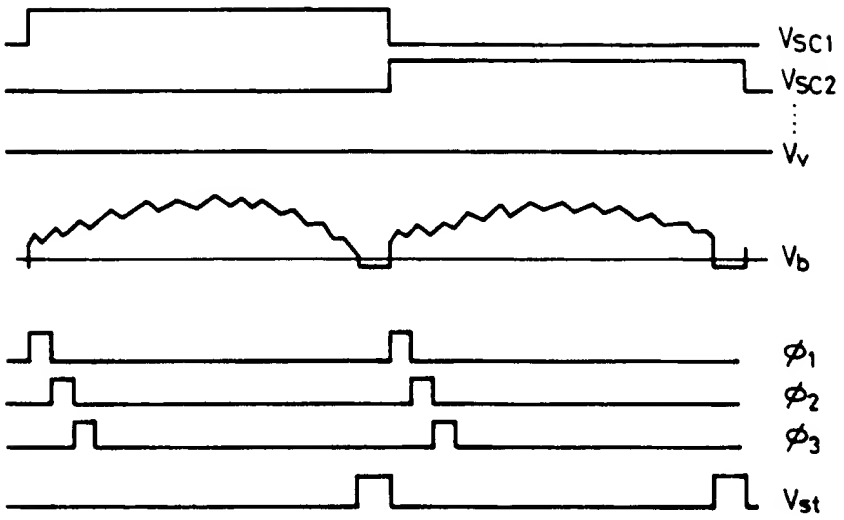


FIG. 6

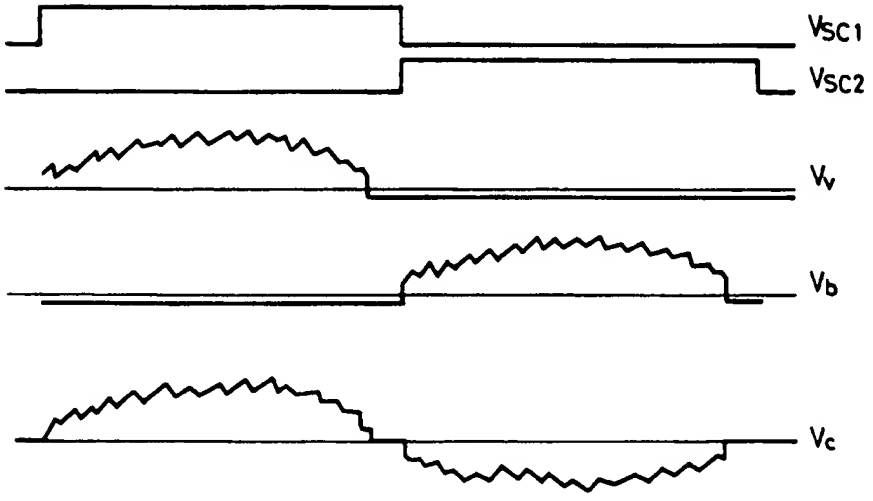


FIG. 7

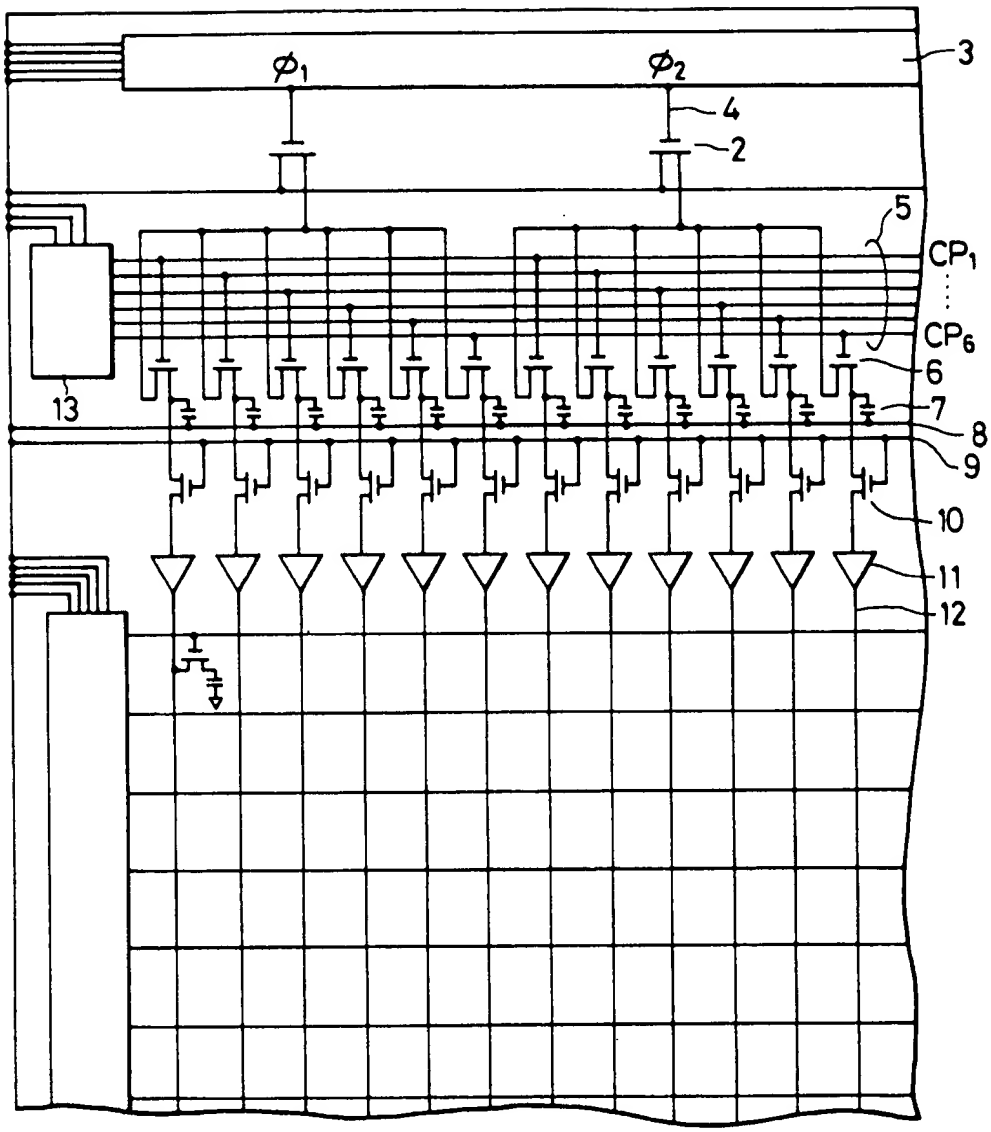


FIG. 8

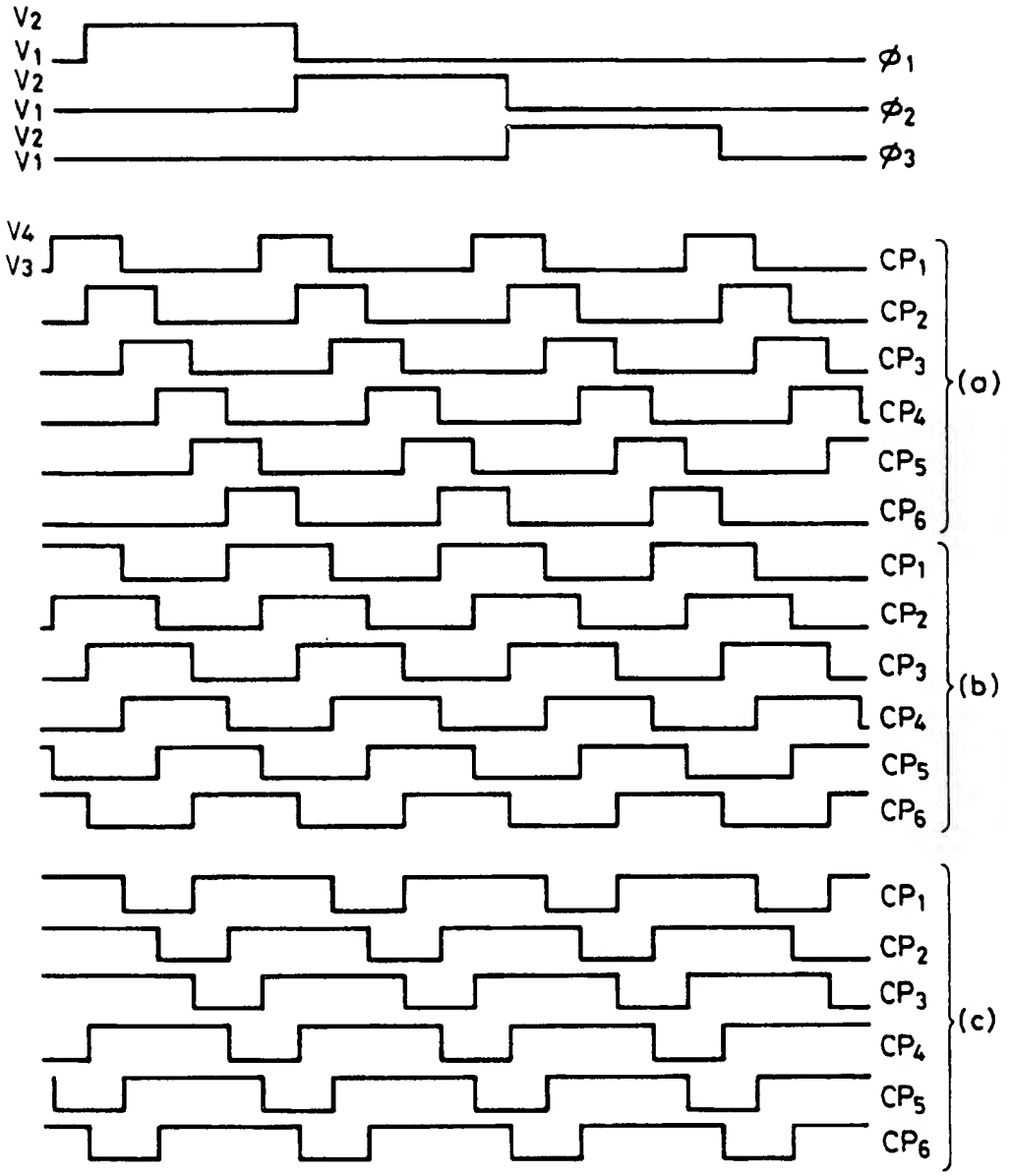

V2
V1
V2
V1
V2
V1
φ1
φ2
φ3
V4
V3
CP1
CP2
CP3
CP4
CP5
CP6
(a)
CP1
CP2
CP3
CP4
CP5
CP6
(b)
CP1
CP2
CP3
CP4
CP5
CP6
(c)

FIG. 9(a)

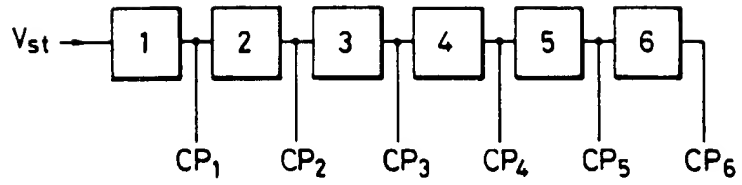


FIG. 9(b)

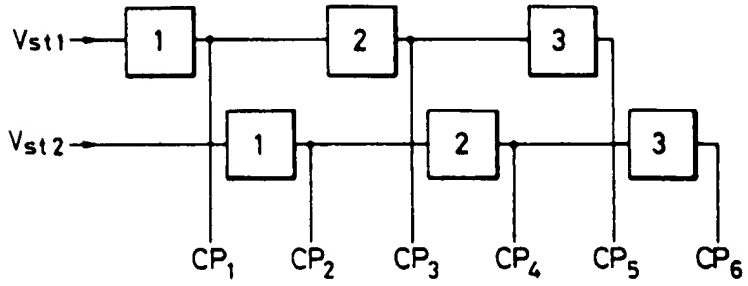


FIG. 9(c)

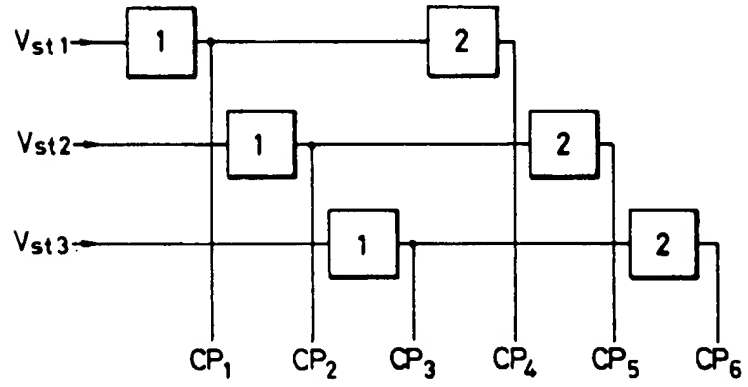


FIG. 10(a)

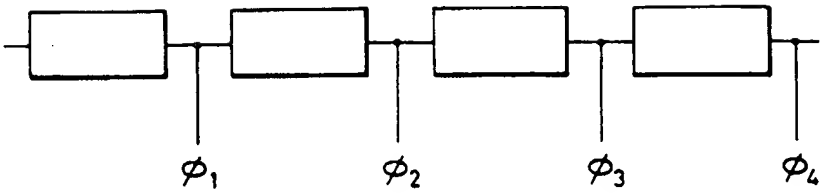


FIG. 10(b)

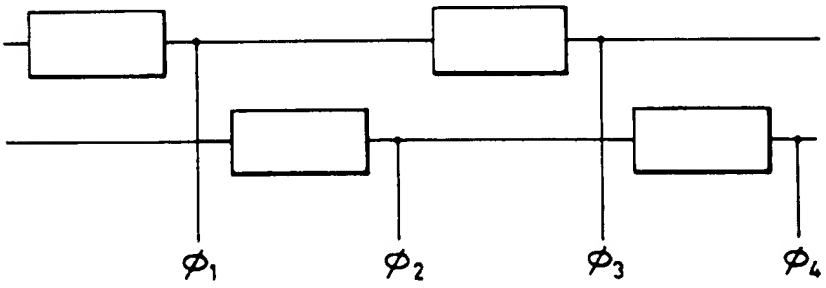


FIG. 11

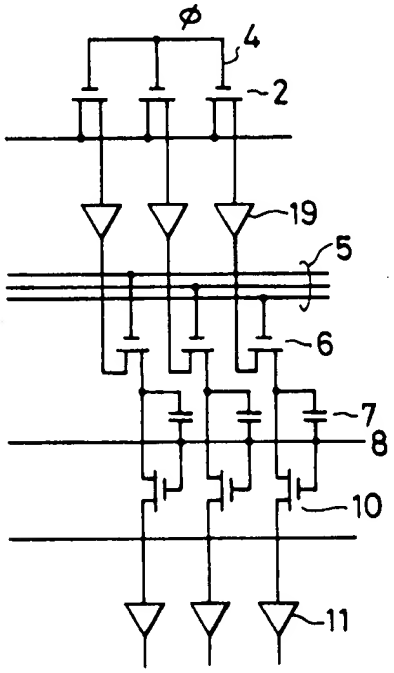


FIG. 12

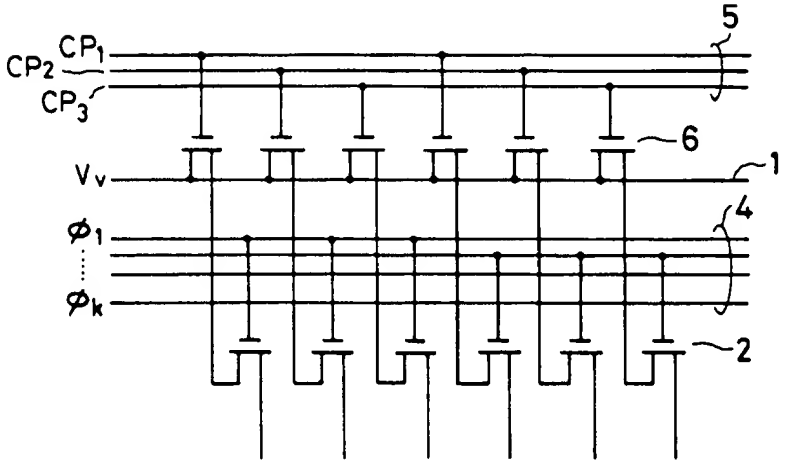


FIG. 13

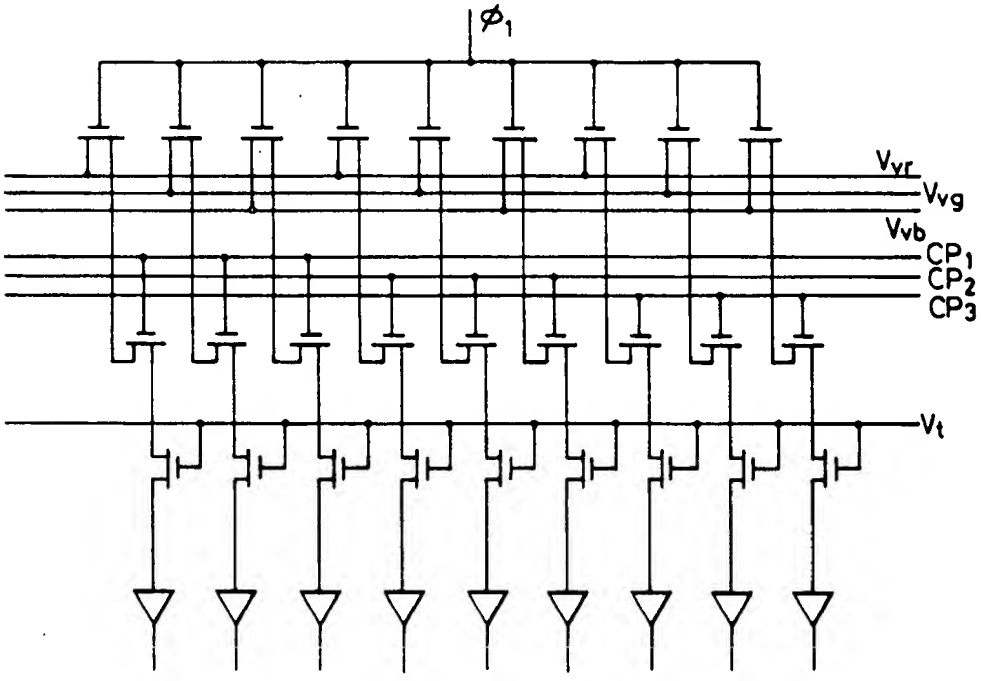


FIG. 14

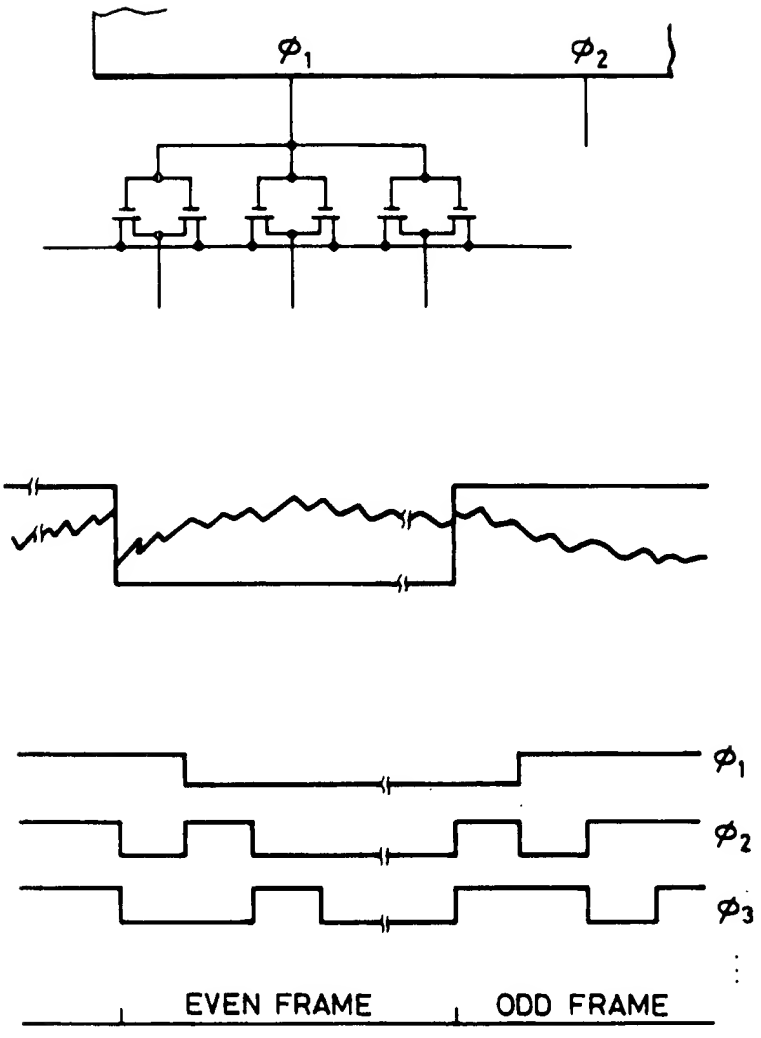


FIG. 15

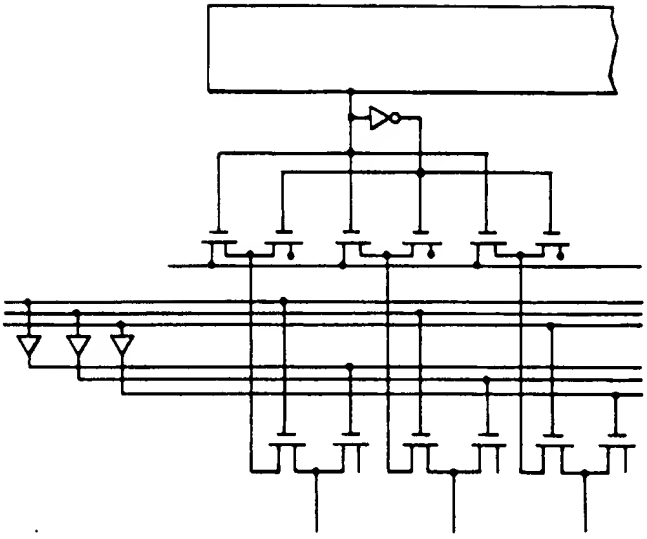


FIG. 16

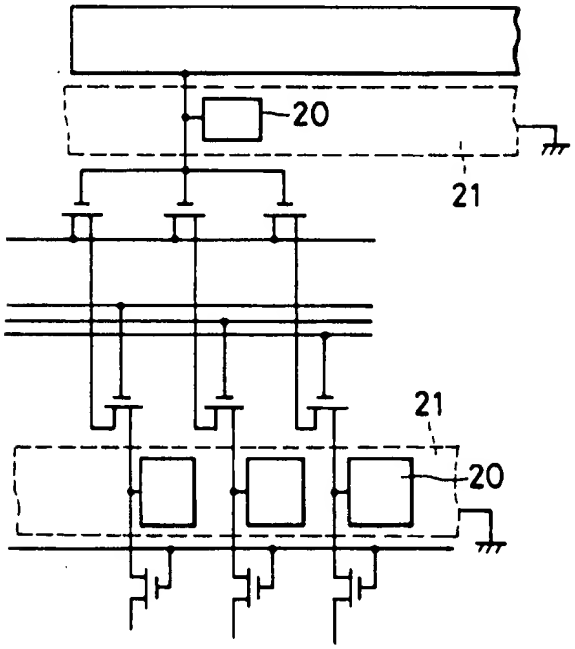
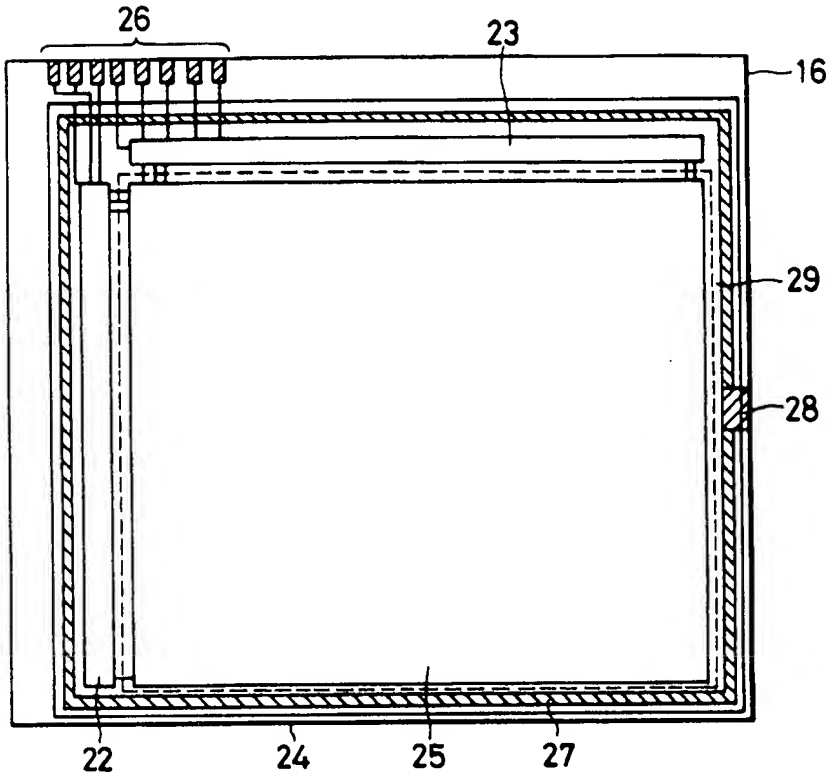


FIG. 17


26
23
16
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22
24
25
27

FIG. 18

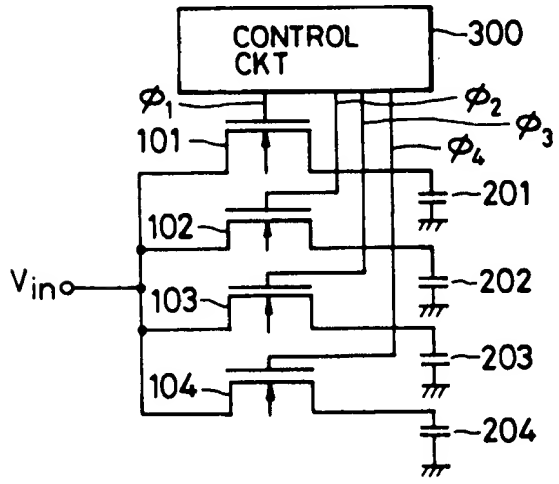

CONTROL CKT
300
ϕ_1
ϕ_2
ϕ_3
ϕ_4
101
102
103
104
V_{in}
201
202
203
204

FIG. 19

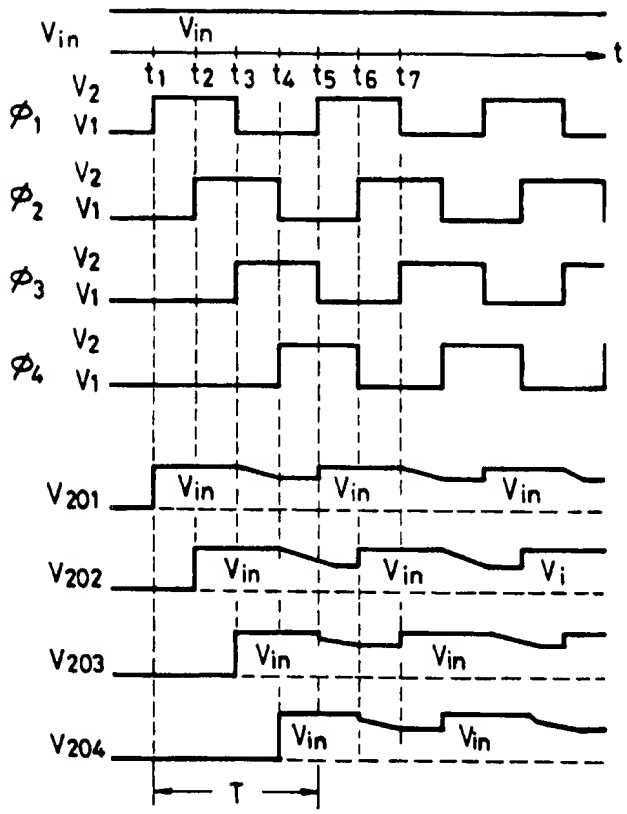

Vin
Vin
t
t1 t2 t3 t4 t5 t6 t7
V2
V1
Φ1
Φ2
Φ3
Φ4
V201
V202
V203
V204
Vin
Vi
T

FIG. 20

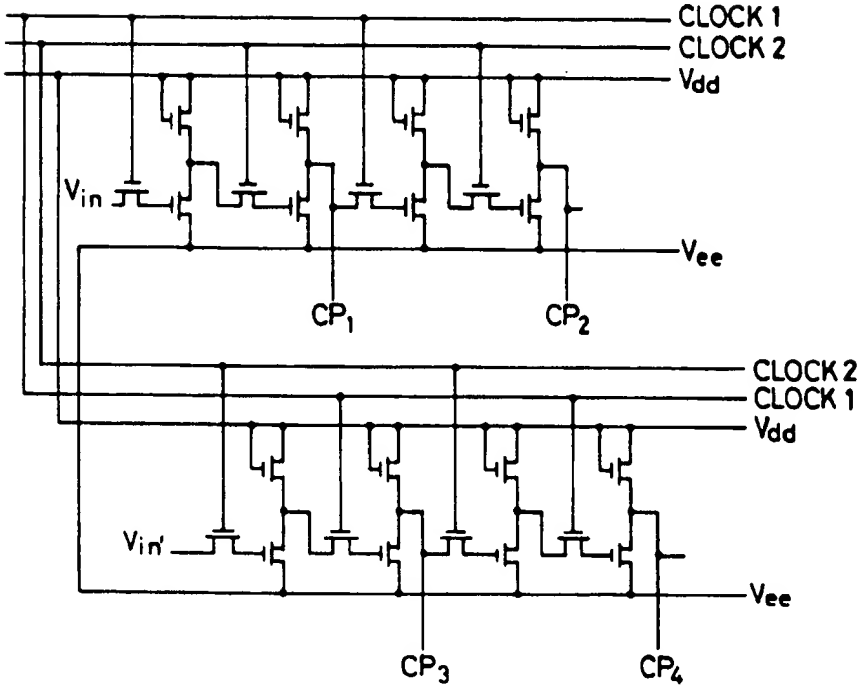

CLOCK 1
CLOCK 2
Vdd
Vin
Vee
CP1
CP2
CLOCK 2
CLOCK 1
Vdd
Vin'
Vee
CP3
CP4

FIG. 21(a)

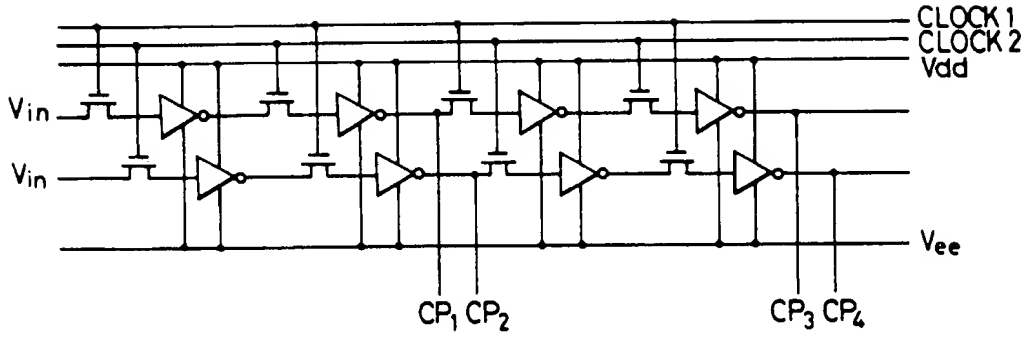


FIG. 21(b)

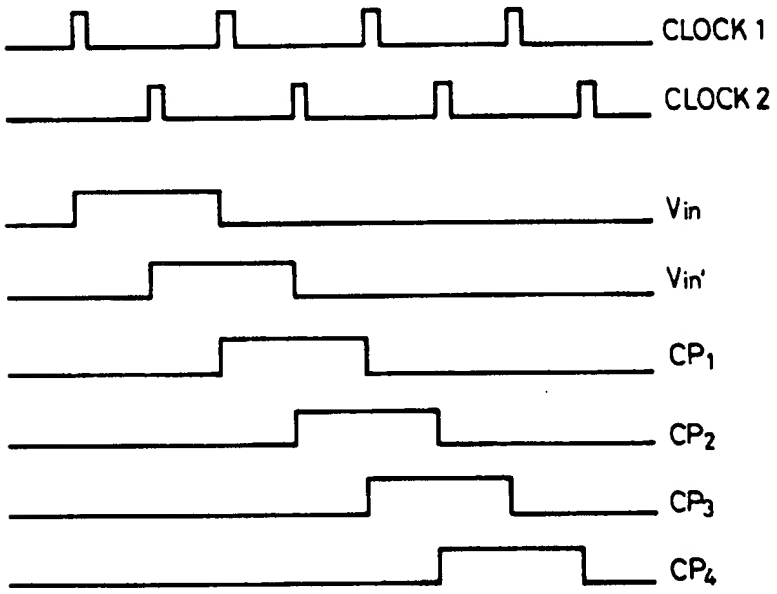


FIG. 22(a)

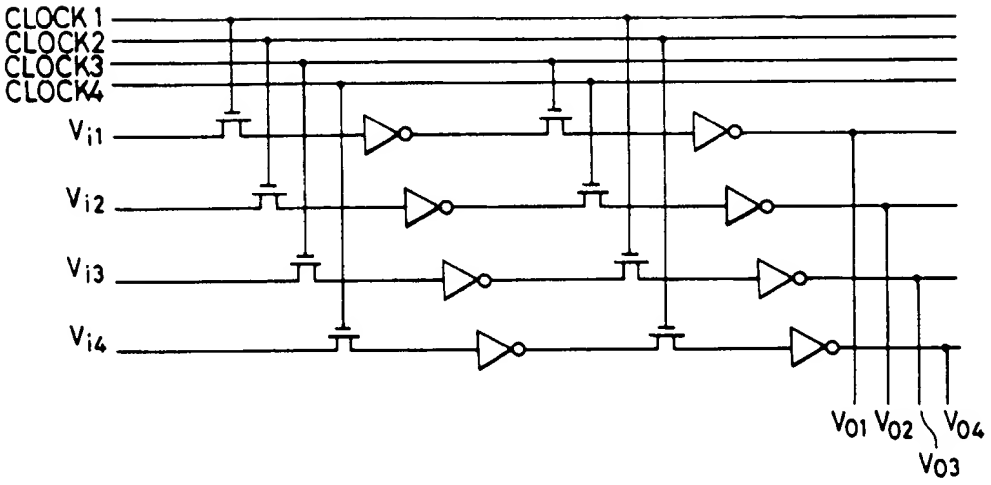


FIG. 22(b)

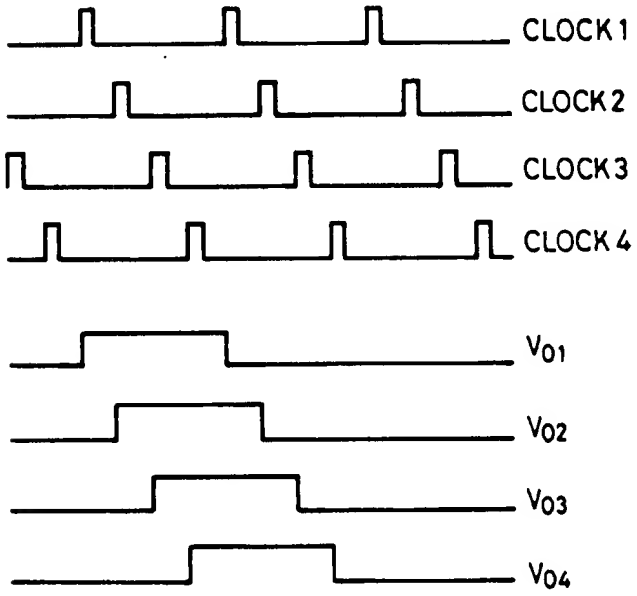


FIG. 23(a)

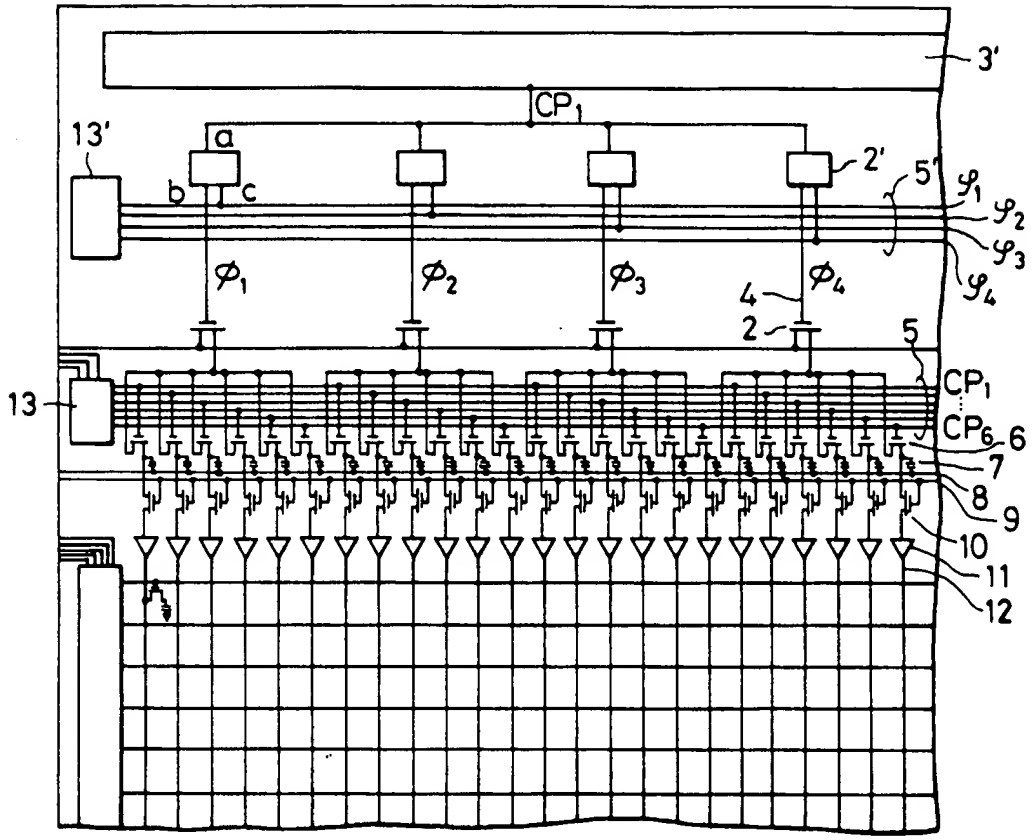


FIG. 23(b)

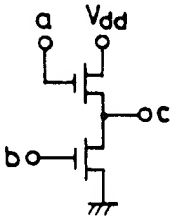


FIG. 23(c)

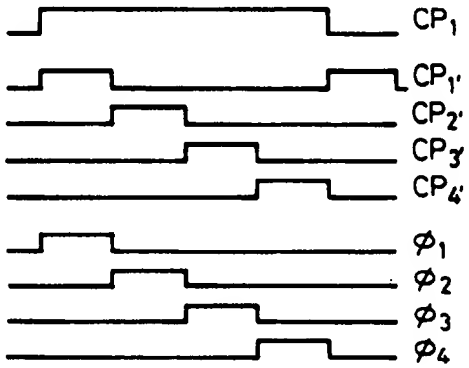
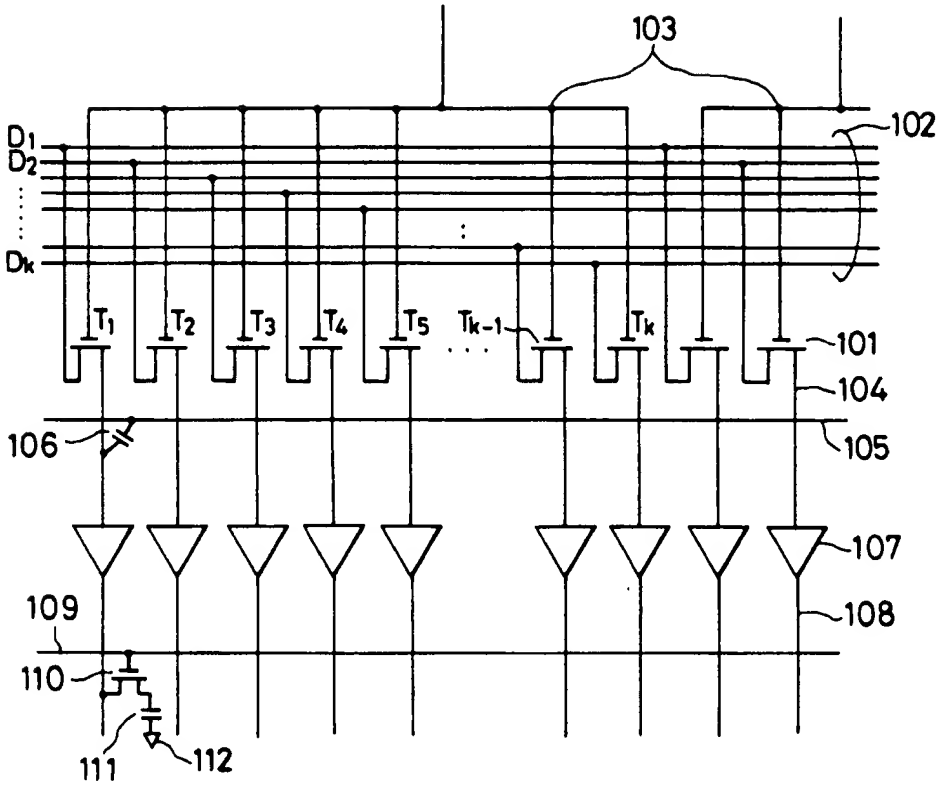


FIG. 24


103
102
D1
D2
Dk
T1
T2
T3
T4
T5
Tk-1
Tk
101
104
106
105
107
109
108
110
111
112